Ultra High Temperature (UHT) Infrared Scene Projector System Development Status

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ABSTRACT

The Ultra High Temperature (UHT) development program will develop, package, and deliver high temperature scene projectors for the U.S. Government. The Infrared Scene Projector (IRSP) systems goals are to be capable of extremely high temperatures, in excess of 2000K, as well as fast frame rates, 500 Hz, and 2 ms rise times. The current status of the pixel design will be discussed with an emphasis on the models developed to facilitate these designs and estimate performance prior to fabrication.

Keywords: Ultra high Temperature, UHT, IRSP, Scene Projection, LFRA, MIRAGE XL, Rise time

1. INTRODUCTION

In an effort to extend the capability of resistive array based infrared scene projectors systems and support the Government's requirements for higher temperature projected scenes, Santa Barbara Infrared (SBIR) has embarked on a unique project to reach higher temperatures with resistive emitter arrays. The Ultra High Temperature (UHT) Infrared Scene Projector (IRSP) program is developing new pixels that can reach the high apparent temperature needs of today's test applications. The technology used to produce the emitter array as well as the drive electronics were leveraged from the existing MIRAGE XL and OASIS 1024 Infrared Scene Projection Systems. These new materials and pixels are being development, with RTI International under the Ultra High Temperature program. This project is being funded by the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the U.S. Army Program Executive Office for Simulation, Training and Instrumentations (PEO STRI). Two complete Ultra High Temperature Infrared Scene Projection systems will be delivered as part of the UHT program, the first of these systems are scheduled to be delivered in the summer of 2013.

The UHT program has been divided into three phases of development. Phase 1, currently underway, focuses on the materials needed to attain apparent temperatures of 2000K and higher. Coupled with the material development is the physical design of the pixel. The pixel's shape and structure determine the rise and fall time as well as the apparent temperature. Phase 1 will develop multiple candidate pixels designs. Each of these pixel designs will be fabricated and tested. The most promising designs will be carried forward into the next phase of the program. In addition to the pixel designs, various test structures will be developed to determine thermal, mechanical, and electrical behavior of the new materials, providing important information for improving UHT pixel models and pixel designs.

The second phase of the UHT program will take the 8 most promising designs from Phase 1 and build them into emitter arrays. Matched to these emitter arrays will be new drive electronics. The drive electronics will consist of a set of Command and Control Electronics (C&CE) as well as a Thermal Support System (TSS). The C&CE will be derived from the PC based Array Control Electronics (PACE) electronics developed for the OASIS1024[1] program.

The third and final phase of the UHT program will take the highest performing pixel design from Phase 2 and build a complete scene projector system around it. The pixel design will have passed through two down selections by this point and will be the best design for the UHT application. The 512x512 emitter array provided with the system will be made from a single pixel type.

The UHT system, as with its MIRAGE XL[2] predecessor, is a turnkey system including all necessary equipment to project high-fidelity infrared scenes. Leveraging the existing MIRAGE XL system technology[3] will allow existing users in the community to easily upgrade to greater performance provided by the UHT system. By utilizing the Command and Control Electronics (C&CE), Thermal Support System (TSS) hardware as well as the Digital Emitter Engine (DEE) architecture, the UHT system will utilize the same electrical and mechanical interfaces as Mirage XL. The C&CE provides the digital scene data inputs for the system as well as overall control of the CSE, TSS and DEE, which is all controlled through a convenient graphical user interface. The C&CE also provides a means for non-uniformity correction of the array, real-time translation and rotation, convolution and global look up tables. Further listing of features can be seen in Table 1.

Table 1. UHT system requirements and features

Parameter	Program Goal
Apparent Temperature Range (K) MWIR (3-5µm)	Cryo – 2000K
Spectral Range	3-14µm
Address Rate (full frame)	500Hz
Windows per array (Targets)	10
Windowing address rate	1kHz
Windowing Size	4x4
Digital Resolution	14 bits
Operability (before NUC)	99.7%
Uniformity (after NUC)	2%
Array Size	512x512
Spatial Resolution (pitch)	48 micron
Operating Temperature	50K to 300K

2. PROGRAM STRUCTURE

2.1 Phase 1. Breadboard Test Structures

During the first phase of the UHT program, SBIR in conjunction with their contractors will be developing high temperature materials and pixel structures. Multiple materials, picked to achieve high temperature, for the pixel will be tested in order to select candidates to fabricate. Additionally, multiple pixel structures will be evaluated via statistical modeling to select the best pixel design for fabrication. Ten to twenty emitter structure and material combinations will be fabricated and tested in this phase, up to eight designs will be chosen at Preliminary Design Review (PDR) for further development and testing in Phase 2.

SBIR is developing and analyzing emitter structures to understand their behavior when heated to temperatures above 2000K. The UHT pixel designs and material sets will need to attain these extremely high temperatures without irreversible mechanical deformation or changes in performance. Test structure will be produced for performance

evaluation at a breadboard level. The results of which will be used to anchor the parameters used in finite element analysis, and to determine failure modes of the pixels. The tests at the breadboard pixel level will include; rise time, maximum apparent temperature, annealing characteristics as well as pixel lifetime.

The materials chosen for pixel fabrication will undergo testing at the thin film level on silicon substrates. This will closely match the silicon Read In Integrated Circuit (RIIC) used in the emitter array for future phases. This testing will include film survivability at the high temperatures as well as testing to verify that the film can be used as part of the normal pixel manufacturing process.

This first phase of the program will end with a Preliminary Design Review (PDR) for the project stake holders where the program will be reviewed and up to eight emitter structures will be chosen to be carried forward for further development and testing in Phase 2. Additionally, during this phase SBIR will be performing a trade study evaluating how to proceed from the current state of the art 512x512 emitters to larger devices. The larger arrays include 1024x1024, 2048x2048, 2560 x 2560 and 4096 x 4096 formats. SBIR will evaluate different manufacturing techniques for the emitter and the RIIC as well as novel packaging approach that may have effects at the system level.

2.2 Phase 2. 512x512 Brass-board Electronics and Tiled Test Arrays

In the second Phase of the program the emitter structures that were down-selected at the PDR concluded in Phase 1, will be tiled onto 512x512 arrays. The arrays will use the NOVA-15 Read In Integrated Circuit (RIIC) from Nova Sensors. This is meant that sub-arrays of the various emitter structures shall be fabricated onto a single 512x512 RIIC. For example, if there were eight emitter structure types carried forward they could be tiled so that each type covered a 128x256 pixel region of a 512x512 array, as shown in Figure 1. The tiled array will allow for testing parameters such as operability and uniformity.

In addition to the emitter pixels being fabricated during Phase 2, SBIR will produce one brass-board IRSP system for use as an ambient or cryogenic test system. The packaged emitter arrays will be capable of being installed in a Dewar based on the SBIR-standard packages used for the MIRAGE XL IRSP systems. The completed Digital Emitter Engine (DEE) consists of a Dewar and close support electronics, will be used for subsequent test and integration of 512x512 brass-board arrays. One packaged array shall be chosen as the pathfinder for integration and test and the other shall be chosen as a “best” deliverable array.

This complete IRSP system will include the necessary control electronics and thermal management system required to make a turn key system. This turn key system will be demonstrated at a government test facility in order to support advanced scene projection with high fidelity, high apparent temperature scenes required by today’s test applications.

The brass-board IRSP system will be operable at 500 Hz frame rates and support a windowing mode for faster frame rates. The system will provide for 10 or more independent windows up to 4x4 pixels and with a refresh rate within those windows of 1 KHz.. At least one of the emitter structure types will be selected to have a 2 ms 10% to 90% rise time and maximum apparent temperature of 2000K with a goal of 2700K or greater.

This phase will conclude with a “graduation” demonstration of the brass-board system at a Government test facility followed by a Critical Design Review (CDR) at which the program shall be reviewed and test data shall be presented on the four to eight emitter structure types fabricated and tested in this phase. At CDR, the best emitter structure will be down-selected for fabrication in Phase 3.

128x256 block of emitter type 1	128x256 block of emitter type 2	128x256 block of emitter type 3	128x256 block of emitter type 4
128x256 block of emitter type 5	128x256 block of emitter type 6	128x256 block of emitter type 7	128x256 block of emitter type 8

Figure 1. 512x512 tiled emitter to be delivered in Phase 2

2.3 Phase 3. 512x512 Prototype Electronics and Arrays

In the third and final phase of the program, the final emitter structure, down selected at CDR of Phase 2, will be fabricated on 512x512 pixel NOVA-15 RIICs and integrated into a turn key IRSP system. The IRSP prototype system will include a packaged emitter array, control electronics and thermal management system. This turn key system will be in addition to the brass-board produced in Phase 2 for use as an ambient or cryogenic test system. Three additional packaged arrays will be fabricated as part of this Phase. The emitter arrays fabricated for this phase will be of a single type. Based on the down selection process started in Phase 1 and carried into phase 2, the final emitter design will have undergone significant testing and process improvement.

The third and final phase of the program will conclude with a "graduation" demonstration of the prototype system, followed by a final program review at which test data will be presented on system performance, lessons learned and the path forward to higher performance and higher resolution systems.

3. PHASE 1 PROGRESS

The UHT pixel architecture was designed to address the key specifications of 2000K MWIR Maximum Apparent Temperature and 2ms rise time. In order to meet these two requirements simultaneously, SBIR has designed several pixels with a range of leg lengths as well as placements within the pixel itself. In addition to the various leg designs the pixel body has been varied to attain the optimum use of the absorber without risk of warping. The UHT program has extensively used detailed pixel analysis and modeling. Potential pixels have been modeled and run through finite element analysis (FEA). FEA predicts whether a pixel will survive operation at high temperature without buckling or failure due to thermal stress. By using the FEA with UHT specific material properties, SBIR has been able to eliminate

pixels designs that show a strong potential for mechanical failure at high temperatures. This process of analysis without having to invest the time and resources into fabricating each potential pixel design has allowed non conventional design to be explored. Several potential designs are shown in Figure 2. In all over 20 designs will be committed to fabrication. Each of these designs will be tested as part of Phase 1. The results of these tests will be used to down select several candidates for use in Phase 2, as well as improve the pixel model.

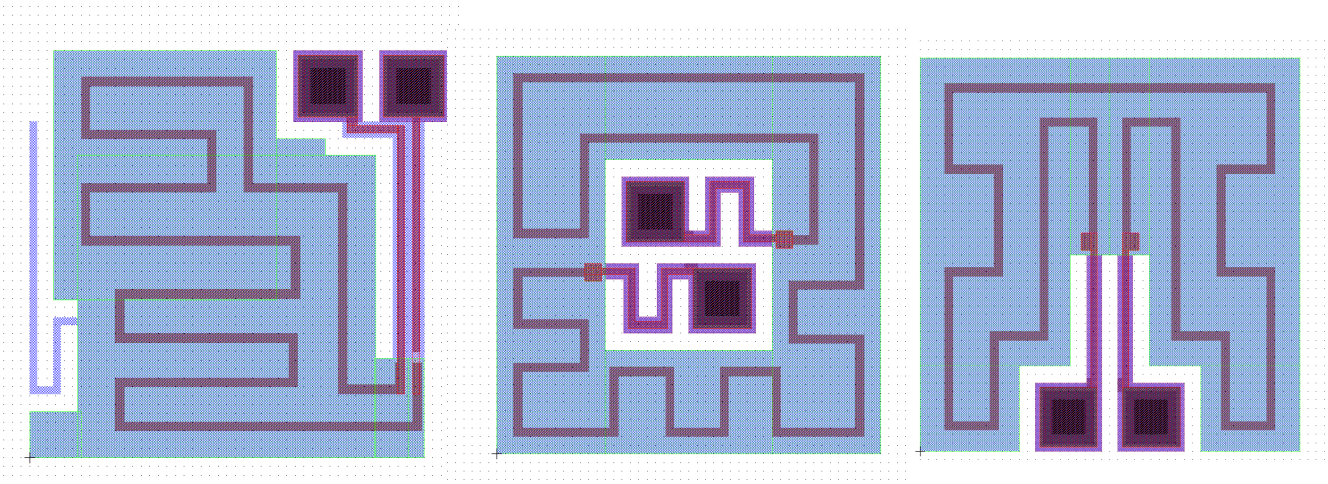

Figure 2. Example of several proposed pixels designs. Left asymmetric legs, center pixel with posts placed at center of pixel body, right pixel has legs placed centrally.

3.1 Emitter Pixel Design and Fabrication

The new pixels designed for the UHT program will have to survive at physical temperatures over 2000K. Accommodating such a high physical temperature is largely a matter of material selection. The temperature difference from the substrate will be greater than 1800K, compared to a 600K difference seen in the current state of the art emitters in use. This large temperature difference leads to some interesting design challenges. At the maximum delta temperature, the pixel body will have grown on the order of 1% due to the coefficient of thermal expansion. This large growth leads to very high thermally induced stresses that can cause mechanical failure of the pixel.

By design, resistive array pixels are generally kept as thin as possible to reduce mass and increase response time. At the same time, the pixel area is maximized which imposes limits on leg length and width. These factors, along with ease of manufacture, have led to pixel designs similar to those shown in Figure 3. In these pixels, the legs are about 4 μm which is set by the manufacturing methods used. The pixel bodies are all about 40 μm wide. Large portions of the pixel body have been thinned to minimize the pixel mass. These pixel designs have worked for physical temperatures up to 800K. During the design of some of the pixels shown in Figure 3, another thermally induced failure was recognized. Because the pixels have a high aspect ratio, meaning they are much thinner than they are wide, they can succumb to buckling. Any that have failed due to buckling can deform enough that part of the active area of the pixel come into contact with the substrate forming a thermal short. This causes effective failure of the pixel as a thermal radiator. The buckled pixel is not permanently deformed, and without other constraints it would return to its initial shape. However, once a pixel comes into contact with the substrate, Van der Waals forces will often hold it there, effectively causing a permanent failure.

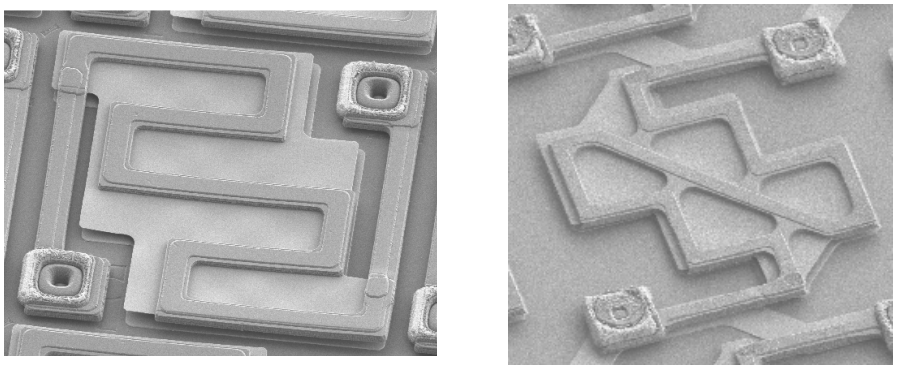

Figure 3. SEM photo of emitter pixels, left MIRAGE XL pixel, right MIRAGE WF[4] pixel The MIRAGE WF pixel is optimized to provide 5ms rise & fall times between ambient and 600K MWIR temperatures.

In order to address the potential failure due to bucking, extensive use of finite element analysis (FEA) was performed during the UHT pixel design. Obtaining material properties at high temperature has been difficult, especially for thin films. In instances where thin film data was available in the literature, it was used. In other cases, bulk properties were assumed as the best estimate. It should be noted that buckling failures are more difficult to analyze than typical yield failures in mechanical structures. Although theoretical buckling loads can be calculated, they are always an upper limit. Most structures will buckle well below their theoretical limit due to imperfections in their fabrication. To accommodate this, a large factor of safety (FOS) is desired if buckling is a possibility. Existing pixel designs were modeled first as a way to validate the FEA models. Designs that had shown evidence of being marginal in earlier testing had the lowest FOS. These pixels exhibited occasional failure at loads about half of that predicted in the buckling analysis. For example, Figure 4 shows the results of a FEA of a marginal pixel design. The plot on the right is a measure of vertical displacement as a function of load. This shows the a the pixel beginning to buckle at a load factor of 1 and displacing enough to form a thermal short at a load factor of about 2. The image on the right is the predicted failure mode which has been observed in the fraction of pixels of this design that failed due to buckling. In order to have margin for manufacturing variations, a minimum FOS of 4, or four times the load at which the FPA predicts it would buckle, was desired for any UHT pixel design. Figure 5 shows a similar analysis of a UHT pixel design. In this case, the pixel warps some but not enough to form a thermal short before exceeding the minimum FOS. The image shown was calculated at a load more than 5 times the expected maximum.

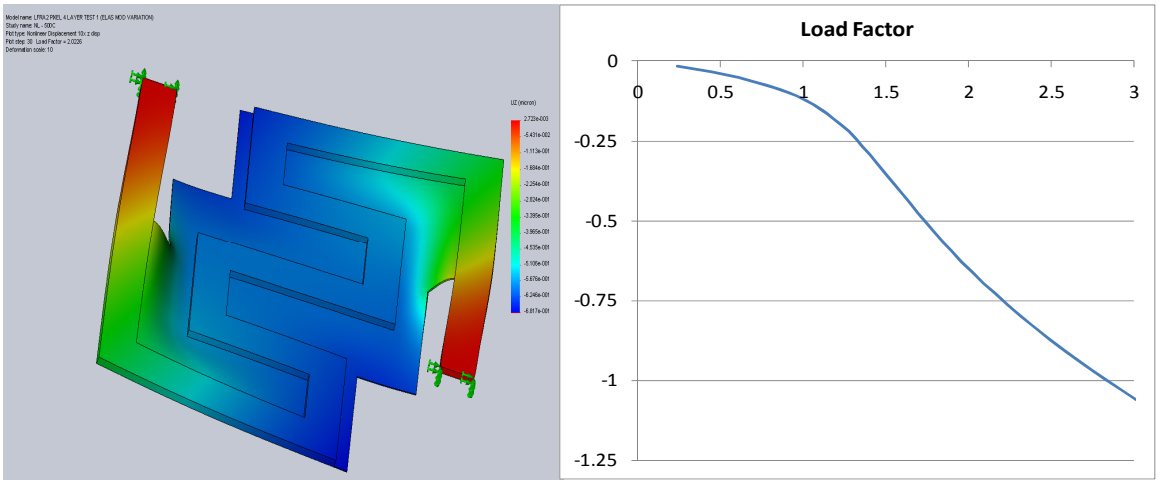

Figure 4. Analysis of a marginal pixel design. The plot on the right shows maximum vertical displacement as a function of load factor. The pixel begins to buckle at a load factor of approximately 1 and would displace enough to touch the substrate at a load factor of approximately 2.5 The image on the right is the predicted failure mode, which has been observed in the fraction of pixels of this design that have failed due to buckling.

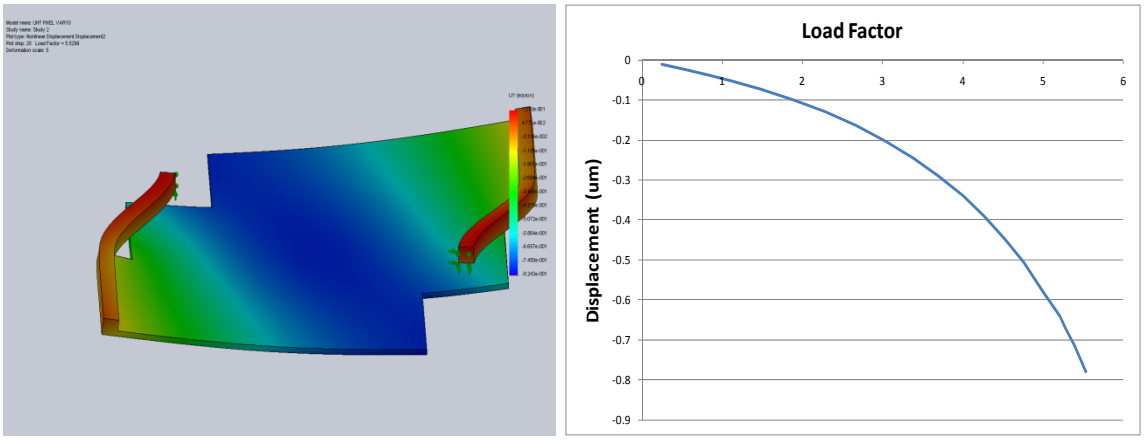

Figure 5. Analysis of potential UHT pixel. The plot on the right is vertical displacement as a function of load factor. The onset of buckling of this design is less pronounced than that shown in Figure 4 above. The image on the left shows the deformed shape at a load factor of 5.5, where the analysis was ended. Even at that load, the modeled pixel would not quite form a thermal short with the substrate. By this analysis, the pixel shown above is an acceptable candidate.

The process was started by analyzing existing designs operated at higher temperature. With triple the temperature change, none of the existing designs were considered acceptable as UHT pixels. All of the pixels suffered from buckling failures. Figure 6 shows an example of a buckling mode failure in an existing pixel design when operated at high temperatures. One of main causes of failure in the pixels was the legs. At 4 µm wide, the legs are relatively stiff and do not flex under the lateral thermally induced load. The 4 µm width was the smallest practical width given the lithographic tools available at the time. Other tools have now come online that can make leg widths on the order of 1 µm practical. Several new designs were proposed to help alleviate the buckling failure predicted at the higher temperatures. In addition to reducing the leg width, its height was increased, which helped improve conductance and increase vertical stiffness. Another series of designs moved the leg contacts into the center of the pixel. This reduced the amount of thermally induced strain the legs need to accommodate. Figure 2 shows a selection of the pixel designs that are being carried forward into the pixel prototype stage of the UHT program. These pixels will be tested for performance and the best pixels will be carried forward into Phase 2 of the program where test arrays will be fabricated to the final pixel selection.

Figure 6. SEM photo of an annealed emitter pixels, left , which has undergone mechanical deformation, right non-annealed pixel, prior to deformation.

4. PREDICTED PERFORMANCE

The UHT program will increase the performance envelope for scene projection systems using resistive arrays. The UHT program will increase the maximum apparent temperature while improving the rise time of the pixels for resistor array IRSP systems. Relative performance can be seen in Figure 7.

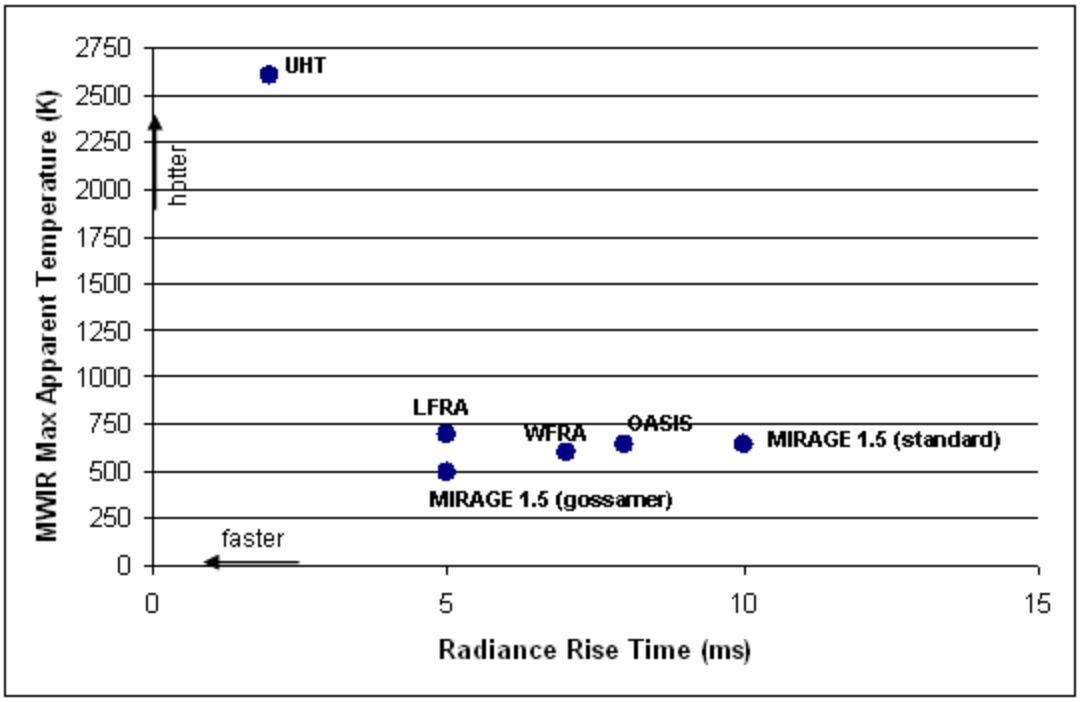

Figure 7. Summary of UHT Array Performance vs legacy emitter programs

5. SUMMARY

Santa Barbara Infrared (SBIR) is developing ultra high temperature emitters for use in state of the art scene projector systems. These systems will leverage existing MIRAGE XL system architecture, but will have significantly enhanced performance. The new pixel mechanical design and materials chosen for the UHT pixels currently under development are predicted to increase the maximum apparent temperature to over 2700K. In addition to the higher temperatures the pixel rise time will also be improved and achieve full transitions in less than 2ms. These advances in IRSP performance are required for test application currently under way and planned in the near future.

DISCLAIMER

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Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Test Resource Management Center (TRMC) and Evaluation/Science & Technology (T&E/S&T) Program and/or the U.S. Army Program Executive Office for Simulation, Training, & Instrumentation (PEO STRI**)**.

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