MIRAGE Dynamic IR Scene Projector Overview and Status

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ABSTRACT

The MIRAGE Dynamic IR Scene Projector is a standard product being developed jointly by Santa Barbara Infrared, Inc. (SBIR) and Indigo Systems Corporation. MIRAGE is a complete IR scene projection system, accepting digital or analog scene data as the input and providing all other electronics, optics and mechanics to project high fidelity dynamic IR scenes to the Unit Under Test (UUT). At the heart of the MIRAGE system is the 512 x 512 microemitter array that incorporates many state-of-the-art features previously not available. The Read-In-Integrated-Circuit (RIIC) leverages technology from IR Focal Plane electronics to provide a system with advanced capability with low risk. The RIIC incorporates on chip DACs, snap-shot frame updating, constant current mode, voltage drive emitters and substrate ground plane providing high resolution and low noise performance in a very small package. The first 512 x 512 microemitter assembly has been received and was imaged on 2 APR 99. The complete MIRAGE system is currently in integration with the first deliverable unit scheduled for June 1999.

Keywords: Infrared, Scene Simulation, Scene Projection and Emitter Array

1. MIRAGE TECHNICAL SYSTEM OVERVIEW

MIRAGE (Multispectral InfraRed Animation Generation Equipment) is a dynamic infrared scene projector system. It is a complete infrared scene projector system with full electronics, emitter assembly and a thermal support subsystem; when coupled with optional collimating optics, the result is a high-fidelity dynamic scene projection system. At the heart of MIRAGE is a 512x512 emitter array, employing key innovations that solving several problems found in previous designs. The read-in integrated circuit (RIIC) features both rolling-update and "snapshot" updating of the entire 512x512 resistive array. This solves the synchronization problems inherent in "rolling-update" only type designs. The MIRAGE custom mixed-signal RIIC accepts digital scene information at its input and using on-board D/A converters and individual unit-cell buffer amplifiers creates accurate analog scene levels. This process eliminates the complexity, noise and speed/dynamic range limitations associated with external generation of analog scene levels.

The proprietary process used to create the advanced technology micro-membrane emitter elements allows for a wide choice of resistor and leg materials, resulting in a highly refined pixel design. This approach to array fabrication also preserves the silicon area under the emitter promoting higher capability in the integrated circuit. With the addition of an update rate of 200Hz, MIRAGE is the most advanced dynamic infrared scene projector system available.

SYSTEM DESCRIPTION
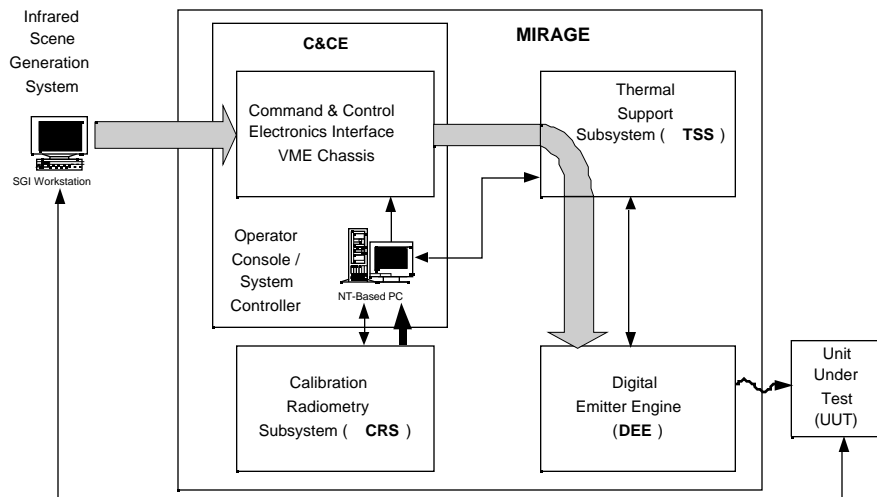
Figure 1. MIRAGE System Block Diagram

The Standard MIRAGE System consists of the following components:

- Digital Emitter Engine (DEE)
    Dewar Assembly
    Close Support Electronics

- Command and Control Electronics (C&CE)
    System Controller PC
    VME Signal Processor Chassis

- Thermal Support System (TSS)

The optional MIRAGE Assemblies are:

- Optical Collimator Assembly
    Collimator

FMS Mechanical Interface

- Calibration Radiometry System (CRS)

2. MIRAGE SYSTEM DESCRIPTION

### 2.1 DIGITAL EMITTER ENGINE

MIRAGE DIGITAL EMITTER ENGINE
Side view of the DEE   **Front view showing chip**

The Digital Emitter Engine (DEE), with its advanced micro-emitter array, is the heart of the MIRAGE Scene Projector. The MIRAGE state-of-the-art emitter array is constructed of thermally isolated suspended thin film resistor structures fabricated on an advanced sub-micron silicon read-in integrated circuit (RIIC). Several innovations designed into the micro-emitter array make MIRAGE the most advanced turnkey scene projector system available in the world. The emitter is packaged in a custom vacuum package. The DEE interfaces to a custom high performance optical system, specifically tailored to the customer's application. Careful design considerations result in a compact DEE weighing approximately 7 kg (15 lbs) with dimensions of 22.9 cm (9 inches) in diameter by 30.5 cm (12 inches) in length. The base of the DEE contains a kinematic mount allowing optical alignment in five axes as well as easy removal and replacement without optical realignment. All electrical and mechanical connections to the DEE are via quick-connect devices to facilitate removal of the DEE for calibration purposes. The MIRAGE dewar is designed for long vacuum hold times (i.e. weeks or months between vacuum pump-downs) therefore eliminating the need for vacuum pumps or vacuum lines on the flight motion simulator.

EMITTER ARRAY

The micro-emitter array is fabricated using a proprietary hybrid approach that eliminates constraints normally encountered during the fabrication of emitters onto silicon substrates. Rockwell Science Center pioneered this approach, Transfer Thin Film Membrane (TTFM). The TTFM process allows for the use of a wide variety of emitter and leg materials and high processing temperatures not compatible with silicon substrates. The emitters are bulk annealed at temperatures (950^OC) that are well above the operational temperatures. This annealing process produces resistors that are very stable both mechanically
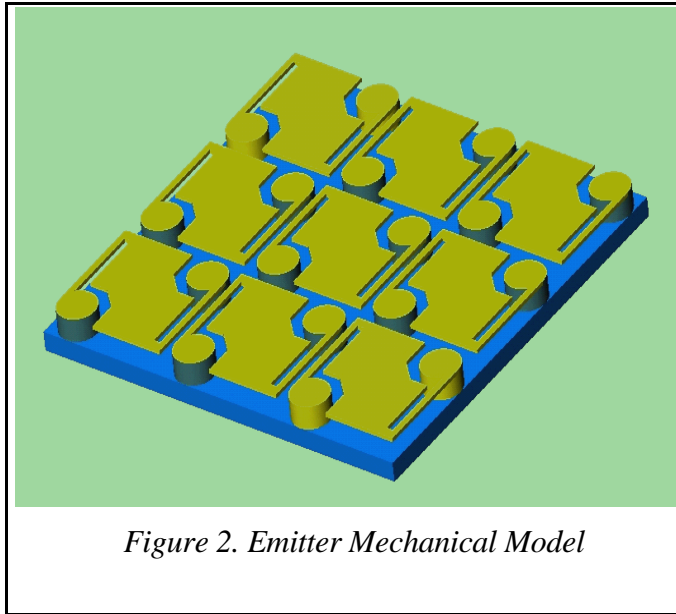
Figure 2. Emitter Mechanical Model

and electrically. The resulting emitters have excellent short-term and long-term thermal stability and are thermally well isolated from the silicon read-in integrated circuit (RIIC.) This thermal isolation allows operation over a wide temperature range with low power dissipation, and results in a thermal time constant of 4.6 msec to support up to 200 Hz frame rates. The mechanical configuration of the emitter array preserves the maximum real estate on the silicon RIIC below each emitter, yet provides a fill factor of 46%.

READ-IN INTEGRATED CIRCUIT

Several of the innovations in the MIRAGE design are centered on the read-in integrated circuit (RIIC), the foundation of the emitter array. The RIIC is a new design that draws on advanced focal plane read-out design techniques. This state-of-the-art custom design features a sophisticated, low-power digital interface and low-noise operation. High yields are realized by using advanced, Class 1 clean room, commercially available .6 micron CMOS processing for RIIC fabrication. This is a proven process used extensively in IR focal plane array electronics manufacturing. These RIICs are processed on 8" wafers that hold 44ea. 512 x 512 die per wafer. 6 wafers have been fabricated with an RIIC yield of 87%.

SNAPSHOT UPDATE

Emitter array designs to date sequentially update the analog level in each unit cell; as soon as each pixel's signal level is presented to the RIIC, that level is immediately
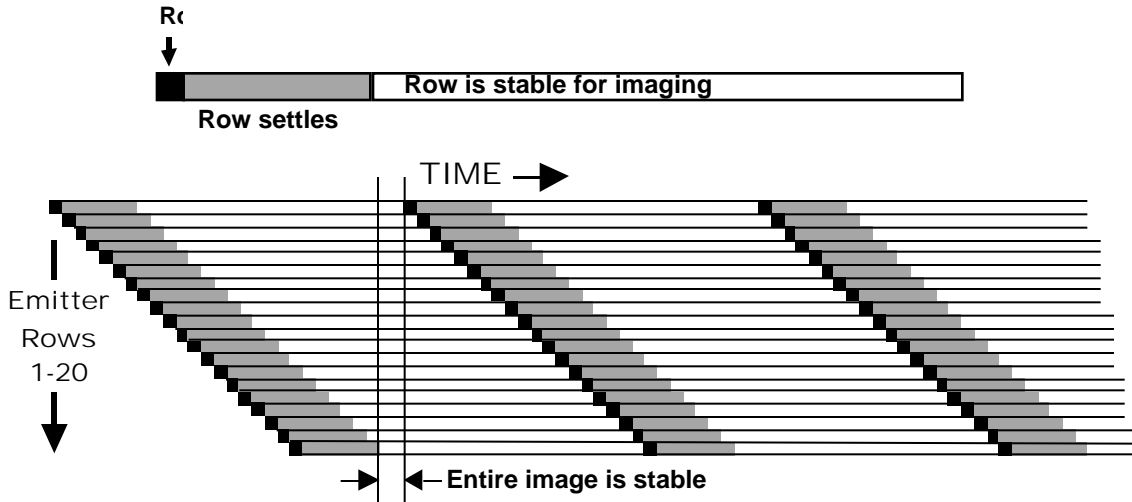
Figure 3. Operation of a theoretical 20-row rolling read-in emitter array at relatively low frame rate. Note the short time period during which each image is stable on the array.

transferred to the emitter. This has the effect that during the time a new image is being read into the array, different emitters on the array will be changing intensity and settling to new levels at different times. At low frame rates, this significantly limits the amount of time that a settled, unchanging image can be presented to a unit-under-test, as shown in Figure 3.

As the frame rate increases, the period when the entire image is stable disappears completely, as shown in Figure 4.
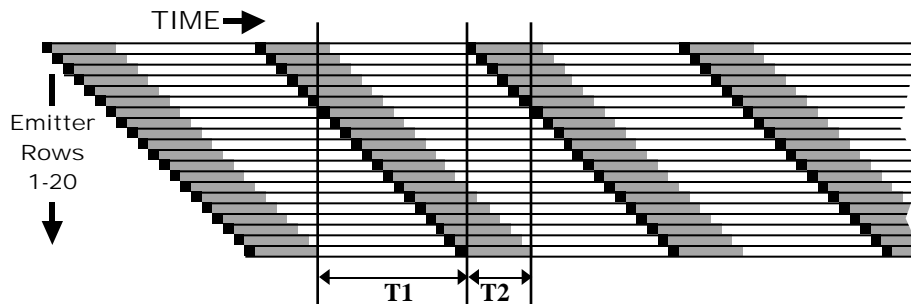

Fi gure 4. Op erat ion of th e 20 -row ro llin g re ad-i n em itte r ar ray at a hi gher fr ame ra te. No te th at th ere is no ti me wh en th e em itte r ar ray is pr esen ting a st able im age.

Note that at any instant during time period T1, the lower rows of the emitter are still displaying intensities from the previous frame, even as the intensities from the current frame are reading in and settling. During time period T2, even as the lower rows of the "current" frame are still settling, levels on the upper rows are already changing to display the data from the next frame. Thus, although this example system may be able to read in

scene data at higher frame rates, there is no time during which the unit-under-test can observe an unchanging, settled image.

To eliminate this constraint on higher-speed operation, the RIIC for the MIRAGE emitter array uses a "snapshot" architecture. All pixels on the emitter array change and settle simultaneously, maximizing the time during which the displayed image is stable - even at the highest frame rate - and greatly simplifying the task of synchronizing the scene simulator to the unit-under-test.
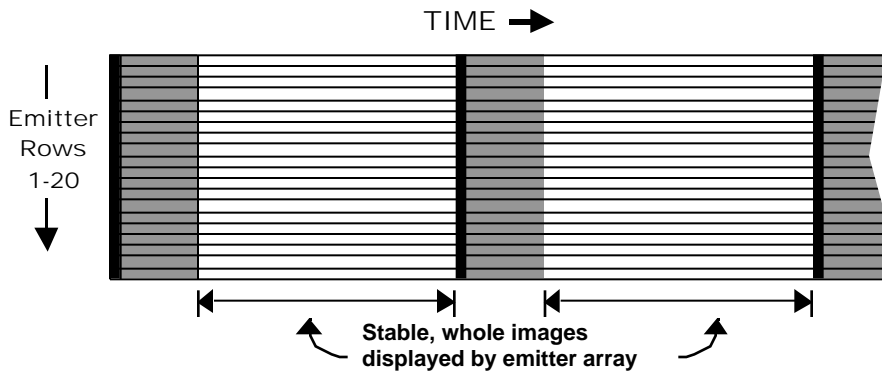

Figure 5. Operation of the snapshot emitter array. All pixels update simultaneously, leaving the maximum possible time for a stable image to be observed by the system-under-test.

Even as the frame rate increases to its maximum value, all pixels will continue to update and settle simultaneously. The snapshot update feature of the MIRAGE array guarantees that image data from different frames will never overlap, as happens with rolling mode arrays.

ON-BOARD D/A CONVERSION AND UNIT-CELL BUFFER

Another significant innovation in the MIRAGE design is the integration of D/A converters (DACs) into the RIIC. Scene projector designs to date have transferred scene intensities to the emitter array using analog inputs; in order to support reasonable refresh rates, multiple analog inputs are used - in some cases as many as 32 or 64. Each input requires an external, precision, high-speed analog source - usually specialized DAC modules - adding to system complexity; the associated cabling and interconnects compromise signal fidelity and noise performance. As emitter array formats get larger, the size and complexity of this external support electronics must grow rapidly in order to maintain reasonable refresh rates. These analog electronics tend to be bulky and must be mounted closely to the emitter array, potentially greatly increasing the mass on the Flight Motion Simulator.

To eliminate these constraints, the MIRAGE RIIC has two on-board, high-speed, precision DACs. These two DACS update the left and right halves of the array and are simultaneously driven by two 16 bit digital busses. This results in a robust, high fidelity digital signal path from the external scene generator electronics to the emitter array. The

entire data path from the C&CE to the emitter array is 16-bits wide, allowing for fast and accurate processing of the digital scene information.

During the read-in of a new image to the emitter array, digital scene data for each row is loaded from the dual 16-bit digital busses into the DACs on the RIIC. The resulting analog levels are then transferred to the unit cells for that row. The RIIC on-chip DACs, operating at 26 MHz, support digital input rates greater than 28 Mega-words per second on each channel, allowing the entire array to be updated in 5 ms (frame rate of 200 Hz).

The pixel unit cell resistor drive circuit is specifically designed to mitigate the effects of mixed-signal (digital and analog) ASIC noise, and to provide excellent (40dB) emitter power supply noise rejection. This power supply rejection capability - localized at each unit cell - along with triple-level metal layers in the RIIC for uniform current distribution, minimizes the output noise and maximizes the dynamic range of the MIRAGE scene simulator.

HIGH THERMAL STABILITY FEATURES

The RIIC incorporates several features that are currently being patented. These features greatly increase thermal stability of the array. Scene dependent non-uniformities, caused by thermal and electrical effects in the emitter and the substrate, are virtually eliminated. These features are:

- Utilizing the emitter substrate as the ground plane- this technique runs the power from the emitter pixels vertically through the substrate to the base of the substrate. By utilizing the base of the substrate as the ground plane, bussbar robbing and electrical crosstalk typical of emitter arrays is eliminated. This also increases the available real estate for the input power bus. This approach provides a more robust design for both the supply and ground planes and greatly enhances scene uniformity and stability.

- Voltage Drive- With current-mode drive, the emitter temperature increases as the fourth power of the input signal. In contrast, with voltage-mode drive the emitter temperature increases as the square of the input signal. As a result, more resolution is available across the temperature range. With the fourth order response, too many bits are used for the low range (bits are lost in noise) while too few bits are available for the balance of the range. Voltage drive provides for higher usable resolution across the range.

- Constant Current Operation- The MIRAGE RIIC incorporates two paths in the unit cell that keeps the total power dissipated in the unit cells constant. The input current is either directed to the emitter or to the shunt path. This approach eliminates electrical crosstalk in the positive power supply. Constant power dissipation allows the two-stage temperature controlled heatsink assembly to be very thermally stable.
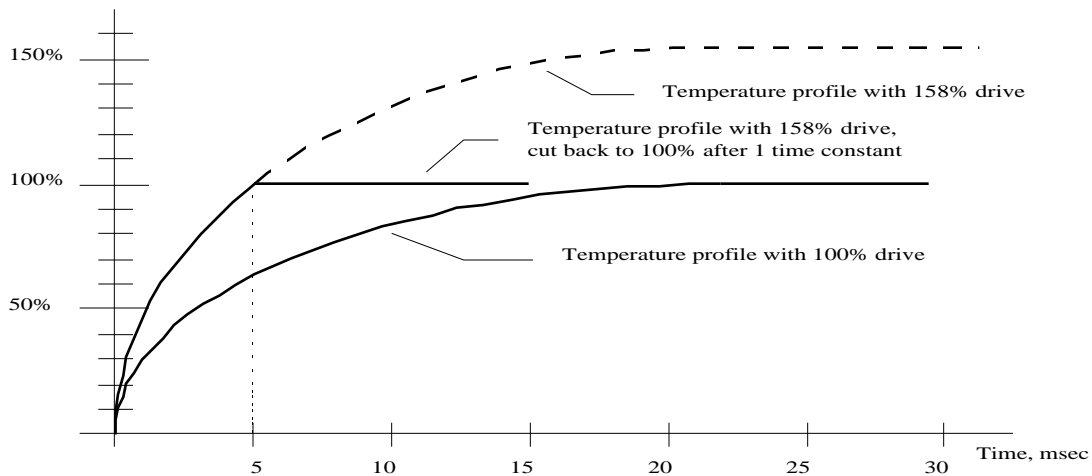
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2.2 COMMAND AND CONTROL ELECTRONICS

The Command and Control Electronics (C&CE) is the signal processor for the MIRAGE Scene Projector. The C&CE has two major electronic subassemblies, the PC System Controller and the VME based signal processor. SBIR has selected Amherst Systems Inc. as its supplier for some of the VME based processing system. This system is capable of the high data rates and complex algorithm execution needed to provide infrared projections for state of the art testing. This C&CE receives rendered scene data from the user scene generation source and drives the micro-emitter array in the DEE. The C&CE sends all of the required commands to the TSS and receives calibration information from the CRS for seamless operation.

The C&CE is built around a commercial power PC array running in the VME chassis and is commanded by a System Controller PC via a Bit 3 interface. The Controller PC, running Windows NT, monitors and controls subsystems via serial communication links and controls the micro-emitter array via the high-speed signal processing subsystem. The signal processing electronics receives rendered scene data from the user's scene generation source or from the optional Digital Playback System, buffers the scene data as necessary, provides non-uniformity correction, time constant enhancement (overdrive), and then supplies an output stream of digital image data to the micro-emitter array. The time constant enhancement algorithm, named the Overdrive Circuit, is a proprietary approach incorporated by SBIR that effectively increases the time constant of the emitter array electrically, without increased thermal mass or increased heat load.

The MIRAGE processing electronics implements a "pixel overdrive" algorithm to improve settling time after a commanded temperature change. Rather than relying on the natural rise time of the pixel to move the temperature to its setpoint, extra power is briefly applied to the pixel to accelerate the temperature change. The following description, while greatly simplified, outlines the principles of pixel overdrive.

With no overdrive, a pixel would reach 63% of its setpoint temperature in 1 time constant. If the pixel is driven to approximately 158% of the change in setpoint (not of the setpoint, but of the change in setpoint), then in one time constant it will reach the new setpoint temperature (within some tolerance). After one time constant, the drive power is set back to its steady state value, to prevent the temperature from rising above its desired setpoint. Graphically, this is how temperature slew will look:

150% — Temperature profile with 158% drive

Temperature profile with 158% drive,
cut back to 100% after 1 time constant

100% —

Temperature profile with 100% drive

50% —

Time, msec

5   10   15   20   25   30

The same principle is used to enhance settling times for a commanded temperature <u>decrease</u>.

With pixel overdrive implemented, the term "time constant" becomes ambiguous in describing settling time, since we are no longer looking at a simple curve.

There are limitations to using overdrive. A <u>large</u> change to a temperature near the limit (either high or low limit) will not have available overhead to allow creation of the overdrive signal. This will not be a problem for <u>small</u> changes from one temperature near the limit to another temperature near the limit. For most activity within the dynamic range of the device, pixel overdrive will yield significant enhancement of settling times.

MIRAGE is designed with low-latency in mind; the C&CE does not need to buffer a full frame of scene data before producing processed emitter output, reducing system latency to a minimum of 49 microseconds from frame input trigger to frame projection.

Rendered scene data from the user's scene generation system enters the signal processing subsystem through a multi-port I/O module, allowing MIRAGE to be configured to accept both analog and digital data in standard formats including: SGI DDO 2, PAL and NTSC. Custom formats can be available by a simple replacement of the I/O module. The emitter data output is provided as a duplex optical fiber using a proprietary high-speed interface. This interconnect allows for very long distances between the C&CE and the DEE with no signal degradation. The output to the DEE is also provided in a standard RS-170 output for viewing of the projected scene on a video monitor. Finally, the C&CE provides control and synchronization input and output signals to allow synchronization of scene generation and projection with the operation of the unit under test.

2.3 PROJECTION OPTICS
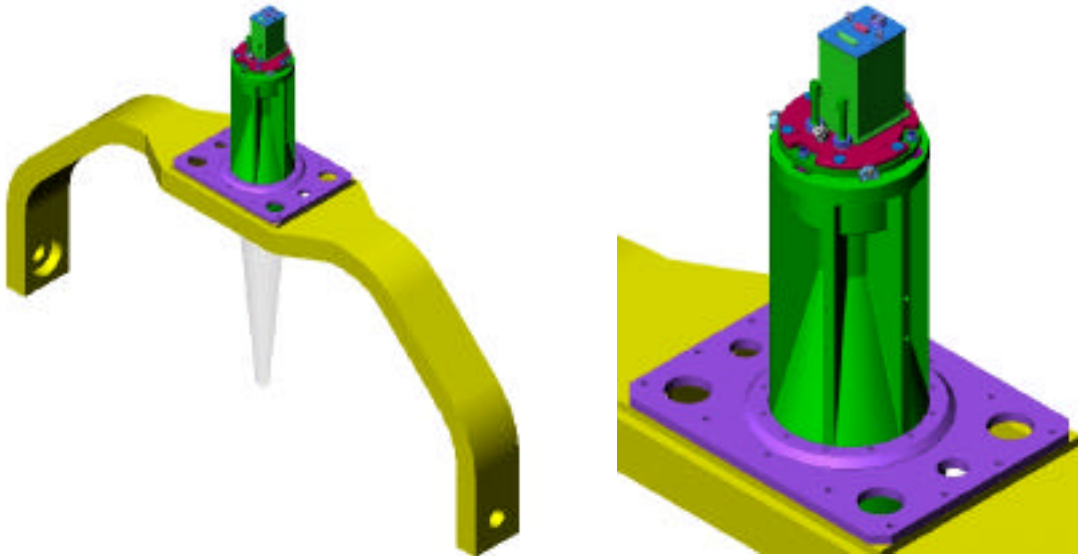
Isometric view of MIRAGE collimator and DEE on the outer axis of the FMS

The Infrared Projection optics are designed to meet the requirements of each application. To select the appropriate collimator system for the application several parameters should be defined. These are: FOV, standoff distance, projected aperture size, mounting configuration and wave band of interest. Many collimator configurations are available and are typically adapted for the specific application. The projection optics will typically be mounted to the flight motion simulator via an adapter plate assembly. The plate will feature alignment pins to accurately position the projector and allow for removal from and reinstallation onto the flight motion simulator. The DEE will be mounted to the optical assembly utilizing a kinematic mount, enabling the DEE to be removed and replaced without realignment. The kinematic mount is a three point mounting system developed by SBIR that precisely and repeatably allows the DEE to be mounted to the optical system at focus. The mechanical mount will be designed to withstand acceleration and shock loads typical of flight motion simulators.

2.4 THERMAL SUPPORT SYSTEM

The Thermal Support System (TSS) is a service unit to the DEE, providing thermal control and power for the emitter array. With the C&CE, the environmental parameters are monitored, providing full system and component protection from unacceptable power, thermal and vacuum values. This subsystem is connected to the DEE with quick connect fittings and connectors, allowing for rapid removal and replacement of the DEE on the flight simulator table or optical bench. Control of the TSS is through the System Controller PC.

Substrate temperature control and uniformity are key elements in the quality of the resulting projected scene. A proprietary control loop design uses feedback from the signal processor in the CSE and from temperature sensors at the emitter array to actively control the substrate temperature within precise limits. The state of the art SBIR Model 920 "Smart" Temperature Controller is implemented for this precision control function.

The TSS also houses high stability power supplies and bias supplies used to run the IR emitter array. All of the above components are housed in a roll-around 19-inch electronics rack for convenient placement in the vicinity of the flight simulator table. Coolant lines, fiber optic and electrical power lines are attached to the TSS via quick-connects; allowing the TSS to be moved away from the UUT without removing cabling from the flight simulator. An additional set of cables will be provided so that the DEE and TSS can be operated on an optical bench or on a calibration bench.

2.5 CALIBRATION RADIOMETRY SYSTEM

The Calibration Radiometry System (CRS) is a highly automated radiometric measurement system, which automatically calibrates the infrared radiation from each pixel of the array. It includes a 320 x 240 MWIR camera, reference blackbodies, optics and positioning mechanics to control the camera's view of the micro-emitter array. The

excellent stability and performance of this radiometric system provides superior performance for non-uniformity correction and calibration. Calibration of the MIRAGE system uses a fully automated, proprietary "step/stare/scan" method, combining image software "micro-scanning" and mechanical "macro-scanning" techniques along with advanced data collection, correlation, and reduction algorithms. Automation of the calibration process reduces the need for operator interaction and enhances the repeatability of the process.

The CRS includes a small stand alone calibration stand with DEE mount, MWIR camera, microscope lens, electro-mechanical positioners, two precision black bodies with controllers and data acquisition hardware.

The MIRAGE calibration sequence is as follows:

1) The DEE is removed from the flight motion simulator using the system quick connects.

2) The TSS is disconnected from the MIRAGE System cabling using quick connects.

3) The DEE is mounted to the CRS and connected to the TSS using the second set of cables supplied with MIRAGE.

4) The calibration process is initiated with commands from the Control PC causing the system to automatically generate the MIRAGE calibration data in table form. The format of this table is a 512X512 array of element correction sub-tables; each consisting of up to 32 entries at 16 bits each. Each of these pixel correction factors will be implemented with 14 bit accuracy in the NUC process during scene generation.

5) After calibration the DEE is reinstalled on the FMS and the TSS reconnected to the DEE support cabling.

This approach to calibration allows a universal calibration system to be used on many types of MIRAGE Array installations, thereby reducing overall cost and system complexity.

3. BUILT IN TEST

Extensive Built-In-Test (BIT) is incorporated in the MIRAGE system. BIT functionality is resident in the C&CE, the CSE and the TSS. BIT is present to protect the system from potential error conditions that could either produce bad results or damage the system. There is a normal operating range, a range that is acceptable for operation but generates a warning, and then a range that will trigger an emergency shutdown.

The C&CE monitors the input digital signal and internal processing. The frame rate and overall processing rates are monitored to insure that processing latency doesn't cause

frame dropout. There are 18 different parameters (bias supplies, reference voltages, and temperatures) monitored by the CSE electronics.

The user interface not only monitors the CSE and C&CE status but also the seven primary parameters maintained by the equipment in the TSS: main emitter power - voltage & current; DEE power supply – voltage & current; dewar vacuum; chiller temperature; and heatsink temperature). The user interface also monitors communication between all the assets and either issues a warning or shuts down operation depending on the severity of communications failure.

4. MIRAGE SYSTEM SPECIFICATIONS

FEATURE	SPECIFICATION
Array Size	512 x 512
Spectral Range	2-14 µm broadband
Pixel Pitch	39 µm
Fill Factor	46%
Array Substrate Temperature	273K
Max. Pixel Temperature	1062K
3-5 µm Effective Temperature*	286K to 780K
8-12 µm Effective Temperature*	286K to 606K
Maximum Frame Rate	200 Hz
Operability	No dead rows or columns, 99.9% operability goal
Temperature Resolution	0.004°C @ 22°C, 0.024°C @ 300°C
Address Modes	Snapshot or Raster
Data Channels	Two 16 Bit Channels
Input Resolution	Up to 16 Bits
Max # Pixels Change per Frame	Full Frame (262,144 pixels)
Data Transfer Rate	Up to 109 Mbytes per second
Max Duty Cycle	Continuous, 100%
System Resolution	All Internal Paths >= 16 Bits
Operating System	Windows NT
Input Scene Formats:	
Digital	SGI DDO2 Standard
Analog	NTSC or PAL Standard
Syncs	Input and Output available
Operating Voltage	205 to 233VAC, 47 to 63Hz

* Assumes 25˚C laboratory temperature; 78% optical throughput.

5. STATUS

The MIRAGE system is currently in final integration. The system has made excellent progress since the announcement of MIRAGE at last years SPIE conference, April 1998. The specific status of the assemblies is:

- DEE
  - Dewar Assembly- The dewar mechanics and electronics are complete. Thermal performance, vacuum hold times and electronic functionality have been tested and operate as expected.
  - Microemitter assembly- The production RIICs are complete and through testing. Full functionality was measured on the RIICs. The first 512 x 512 array with emitters hybridized to the RIIC was received 31 MAR 99. The array was imaged on 2 APR 99 with excellent results! The imagery was run through the entire system, C&CE to fiber optic to CSE to emitter array. Data was collected with an Indigo InSb camera operating in the 3-5 micron waveband.
- C&CE- Most of the control electronics are complete and in integration with the DEE and TSS. The digital and analog interface boards will be ready for integration in May 1999.
- TSS- The Thermal Support System is complete and supporting the integration of the DEE and C&CE.
- CRS- The Calibration Radiometry System is in design and early stages of assembly. The CRS will be complete in June 1999.

Overall the system performance looks very good. Uncorrected uniformity looks excellent. The first system will be ready for delivery in June 1999.

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CORRESPONDENCE

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