MIRAGE: Developments in IRSP Systems, RIIC Design, Emitter Fabrication, and Performance

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ABSTRACT

SBIR's family of MIRAGE infrared scene projection systems is undergoing significant growth and expansion. The first two lots of production IR emitters have completed fabrication at Microelectronics Center of North Carolina/Research and Development Institute (MCNC-RDI), and the next round(s) of emitter production has begun. These latest emitter arrays support programs such as Large Format Resistive Array (LFRA), Optimized Array for Space-based Infrared Simulation (OASIS), MIRAGE 1.5, and MIRAGE II. We present the latest performance data on emitters fabricated at MCNC-RDI, plus integrated system performance on recently completed IRSP systems. Teamed with FLIR Systems/Indigo Operations, SBIR and the Tri-Services IRSP Working Group have completed development of the CMOS Read-In Integrated Circuit (RIIC) portion of the Wide Format Resistive Array (WFRA) program – to extend LFRA performance to a 768 x 1536 "wide screen" projection configuration. WFRA RIIC architecture and performance is presented. Finally, we summarize development of the LFRA Digital Emitter Engine (DEE) and OASIS cryogenic package assemblies, the next-generation Command & Control Electronics (C&CE).

Keywords: Command & Control Electronics, Emitters, IR Scene Projection, LFRA, MEMS Fabrication, MIRAGE 1.5, MIRAGE II, OASIS, WFRA.

1. INTRODUCTION

Design, fabrication, and test of several next-generation resistive emitter-base IRSP systems are in full swing at SBIR. The transition of emitter fabrication from development to production is complete at MCNC-RDI, with future process improvement research ongoing. Handoff from design to manufacturing is underway for upcoming DEE and C&CE subsystems. LFRA, OASIS, WFRA, and MIRAGE II are all expected to produce a variety of new projection RIIC and/or emitter devices for test and evaluation in 2005. In this paper, we provide an update on each of these key technological areas and development programs.

2. EMITTER FOUNDRY

The last year has brought continued successes in emitter array production, packaging, process improvement, and start of production. As described in the following sections, numerous improvements have been made with respect to emitter manufacturability, yield and performance.

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2.1. MIRAGE 1.5 Emitter Fabrication Results

MCNC-RDI completed their second emitter lot (MIRAGE 1.5), which employed the same pixel geometry and layout as was used to validate the transfer of emitter fabrication technology from Honeywell: the ISC 9711 RIIC, 39 μm pixels, 4 gossamer GE dice per wafer, and 4 non-gossamer dice per wafer. Several successful manufacturability improvements were implemented on this run that resulted in an average operability of 99.8% for the eight devices tested to date. We attribute the phenomenal yield to improved mask cleanliness, tight rework criteria, and several process and mask modifications. The performance data matched the predictive model very closely. The results were successful by all measures: performance, yield, knowledge gained, and improvements identified.

The new reflector metal, validated in the phase 2 run, was successfully employed on all MIRAGE 1.5 wafers, with an approximately 5% increase in pixel radiance. The legacy pixel bridge film stack required a complicated and time-consuming deposition process for reasons that are no longer relevant (*i.e.* some of the steps were required for purely historical reasons). One-half of the wafers from the MIRAGE 1.5 fabrication run received a simpler, more manufacturable stack, while the other half were fabricated with the legacy bridge structure. Almost all the devices selected for packaging and testing from this run incorporated the new stack, and no performance degradation was observed. One half of the LFRA wafers and the entire OASIS lot will receive this alternate bridge stack.

2.2. Emitter Fabrication & Process Improvements

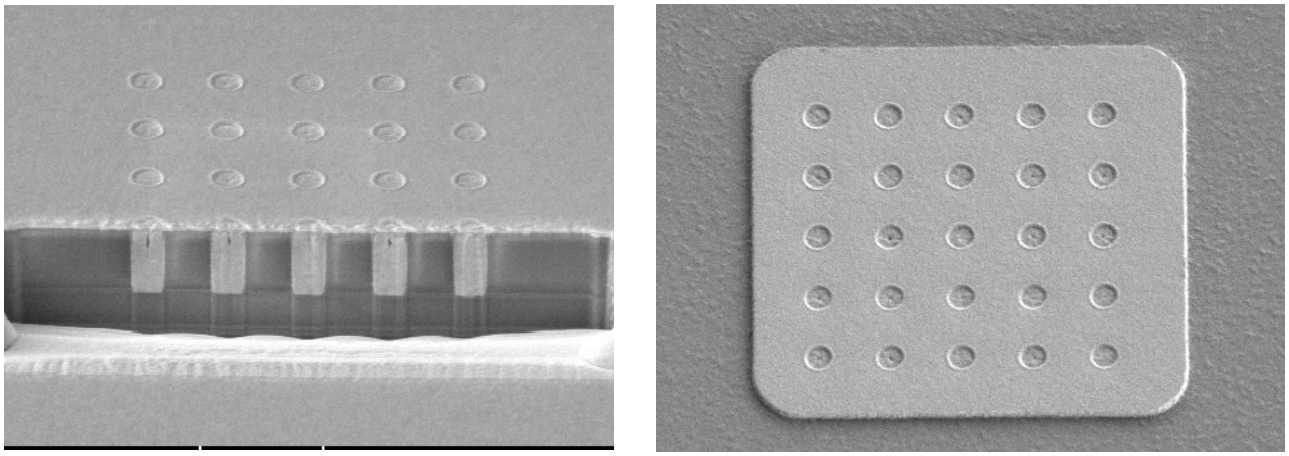
Numerous development tasks were undertaken to improve emitter manufacturability, yield and/or performance. Most of the development tasks discussed below will be implemented in current or planned emitter fabrication runs.

Etch Uniformity – The etch uniformity for a variety of the films comprising the pixel has been improved by more than a factor of two as a result of a tooling modification. This modification also resulted in reduced wafer handing and increased throughput. This improvement is expected to result in enhanced radiance uniformity and has been implemented in the LFRA fabrication run and will be part of all future emitter fabrication runs.

Mask Improvements – Numerous modifications to the emitter mask sets have been implemented: 1) sacrificial layer peeling was eliminated, which resulted in much improved lithography and increased yield, 2) additional alignment targets have provided more flexible alignment capabilities, and 3) a test coupon was designed that will provide insight into a variety of different aspects of emitter fabrication as well as yielding mini-arrays for annealing, future pixel designs and other developmental tasks. A mask review document and process have been devised and put into practice to ensure that the mask set and the planned emitter fabrication processes are consistent with design specifications.

Rework Process – Based on extensive failure analyses from functional devices, the fabrication sources of a variety of classes of defective pixels have been identified. This knowledge enables fabrication personnel to identify defective pixels at the process step responsible for those defects. Based on this capability, a set of rework criteria has been established that resulted in substantially improved pixel operability for the MIRAGE 1.5 run, and will be implemented on all future device fabrication runs.

CMOS Contact – The OASIS program has implemented a major improvement in the CMOS design and layout that supplies the pixel's top metal electrical contacts at the surface of the CMOS via an array of metal posts. Figure 1(a) shows a cross section through one row of the 5 x 5 array of metal posts that connects the CMOS surface to the underlying metal layer. All previous generations of devices (including Honeywell's) had these contacts buried beneath a thick overglass layer, which required planarization (CMP) prior to emitter fabrication, and etching through more than 1 μm of dielectric to make contact to the CMOS circuit. The need for third-party planarization has been eliminated by the new design because the CMOS process is planarized at the top surface of the wafer, rather than below top metal. As-received wafer planarity has been measured and found to be consistent with the requirements of emitter fabrication. Figure 1(b) illustrates the contact pads, which will be deposited and patterned over the posts during emitter fabrication in order to provide a large area for connecting the emitter circuit (*i.e.* there are two such contact pads per pixel). The compatibility of these pads with the subsequent emitter fabrication process was exhaustively evaluated via experiment and found to be compatible with all processes and materials.



(a) (b)

Figure 1 – (a) Cross section illustrating the 5 x 5 CMOS post array connecting the die surface to the underlying metal layer, and (b) contact pad over the post array.

Anneal Experiments – The anneal characteristics of the absorber were measured and found to contribute negligibly to the emissive properties of the pixels for the current generation of devices. Further emitter annealing experiments have been performed in order to identify potential contributions of various fabrication sources to anneal characteristics.

Hot Pixel Removal – SBIR has developed the capability to eliminate "stuck-on" pixels using a laser to cut through the resistor while leaving the pixel structure intact. This can be performed in-situ, without the need to remove the array from the dewar or break the dewar vacuum.

Pixel Release After Attach – IR emitter array pixels are more susceptible to damage from wafer/die handling after the sacrificial layer etch step in the legacy fabrication sequence. To maximize pixel yield, it would be preferable to perform the sacrificial layer etch after the emitter die has been attached to the package, thus reducing the handling of released emitter dice. This development task has been completed and deemed unacceptable due to the low lateral etch rate of the sacrificial layer, leading to extended etch times and eventual damage of the pixel structure.

New Sputter Tool – The primary operability issue associated with emitter fabrication is flaking in the sputter chamber during certain film depositions. The flakes fall onto the wafers at random times during the course of film deposition, and have been directly correlated with inoperable pixel clusters. The configuration of the current generation of sputter tools at MCNC-RDI lends itself to flaking because the wafers sit below the target and shutters, thereby enabling gravity to pull the flakes down towards the wafers. Several workarounds have been devised and implemented in order to minimize the problem, but flakes remain the single biggest known operability issue. MCNC-RDI is in the process of procuring a new, "side-sputter" deposition system that is expected to eradicate the flaking entirely. Furthermore, this tool will be dedicated to emitter fabrication, thereby eliminating any possibility of contamination that might result from non-emitter process materials (*i.e.* other MCNC-RDI programs).

2.3. Current Emitter Fabrication Runs

2.3.1 LFRA Emitter Fabrication

MCNC-RDI is presently fabricating emitters on ten (10) LFRA wafers, incorporating MCNC-RDI's first pixel design and layout (gossamer), and the ISC 0104 RIIC with one die per wafer. One half of these wafers will receive the simple bridge stack discussed previously. Emitter processing is approximately 50% complete at MCNC-RDI. A test coupon has been designed and incorporated into the mask set, which includes numerous in-process fabrication aids (*e.g.* clearing structures and contact chains) as well as a variety of pixel configurations and mechanical structures which will enable

evaluation of alternate designs and future device improvements. Stringent inspection and rework criteria have been established for these devices, which are expected to enhance pixel operability.

2.3.2 OASIS Emitter Fabrication

Ten (10) OASIS wafers are planned to start emitter fabrication in March 2005, incorporating the SB317 RIIC with four dice per wafer. The OASIS RIIC incorporates the metal post arrays illustrated in Figure 1, and will include the contact pad shown in the same figure. The entire lot will incorporate the new bridge stack.

3. LFRA

Over the past year, LFRA has continued its development cycle, and we are approaching integration and test of the first deliverable system.

3.1 LFRA Array Development Status

As mentioned in 2.3.1, emitter fabrication is approximately 50% complete at MCNC-RDI. The LFRA fabrication run started with four-inch CMOS wafer cores, containing a single LFRA RIIC die per wafer. Emitter design and layout have been described at prior conferences, and are optimized for performance and yield.

3.2 LFRA Digital Emitter Engine (DEE) Development

The LFRA DEE design has also been reported previously at SPIE. The final top-level DEE assembly and the highly advanced Multi-Layer Ceramic (MLC) array package are shown in Figure 2.

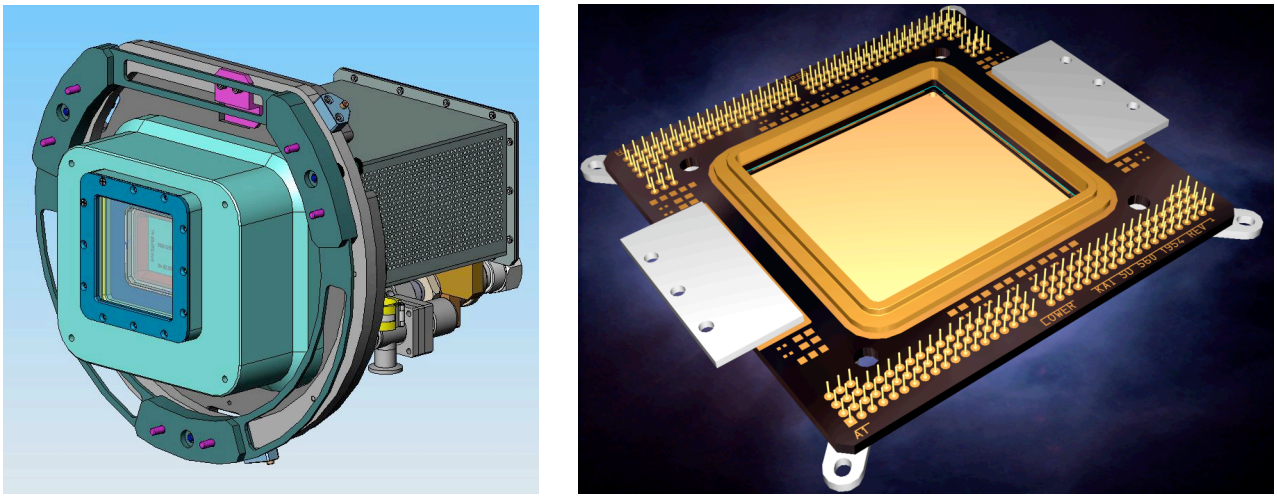


Figure 2 – LFRA DEE (left) and Multi-Layer Ceramic (MLC) Chip Carrier (right)

3.3 LFRA Command & Control Electronics (C&CE) & Thermal Support System (TSS)

The LFRA C&CE, also reported at prior conferences, is in the final stages of hardware and firmware completion. The Translation/Rotation Processor (TRP) and convolution functions are the last major components in design. All other key components have been developed and demonstrated as a part of the initial MIRAGE II deliverables discussed herein. The baseline LFRA C&CE architecture is shown in Figure 3.

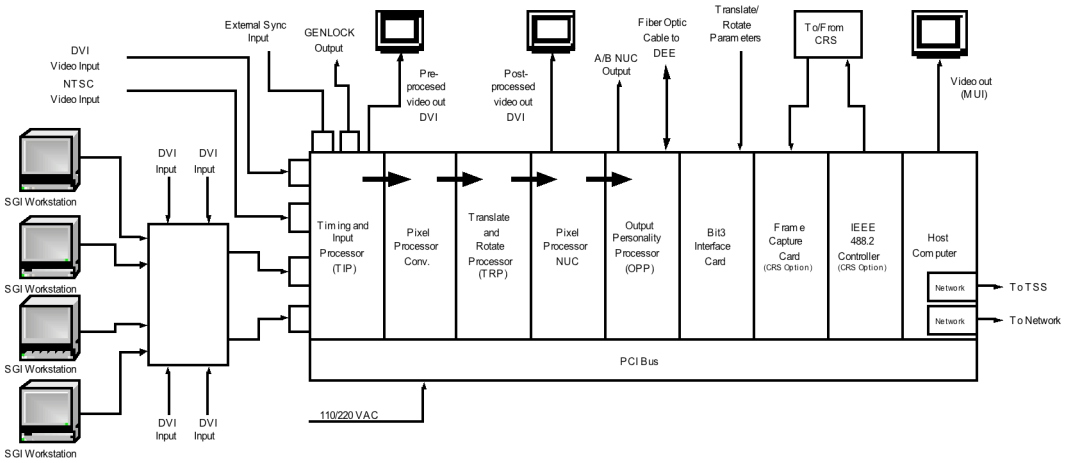


Figure 3 – LFRA C&CE Functional Block Diagram

The LFRA C&CE is packaged into a single 19-inch rack unit, as shown in Figure 4 (left). The Thermal Support System (TSS) includes a high-capacity chiller using HFE7100 coolant, and a rack of power supply, temperature control, vacuum, and monitoring components – as shown in Figure 4 (right).

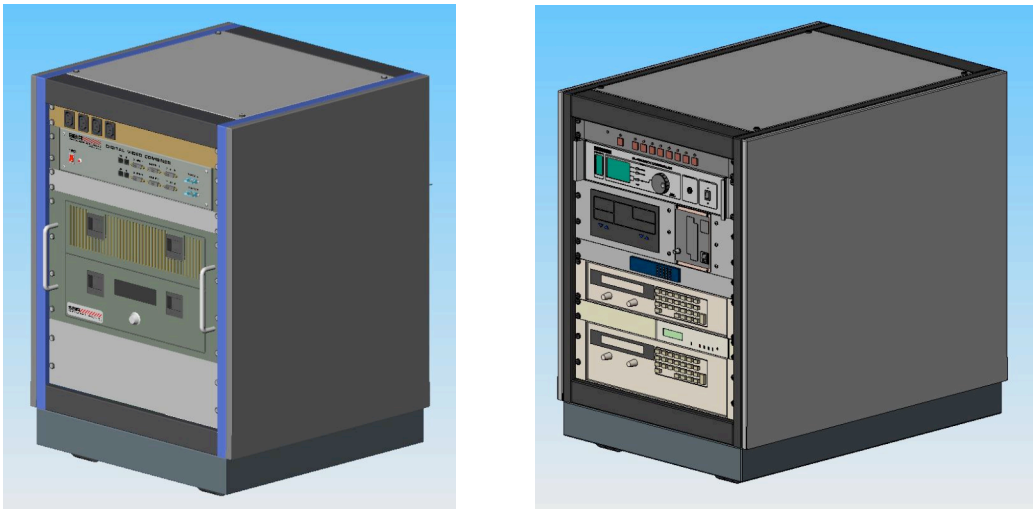


Figure 4 – LFRA C&CE Rack (left) & TSS Rack (right)

At next year's conference, we plan to present top-level IRSP performance data for the first production systems.

4. WFRA

In early 2004, the Tri-Services IRSP working group kicked-off the Wide-Format Resistive Array (WFRA) program, aimed at providing the capability to project wide aspect ratio IR scenes in applications requiring more than 1024 pixels in the horizontal dimension. The resulting 768 x 1536 architecture is currently in development, and utilizes a new, fully custom RIIC, enhanced LFRA DEE, and updated C&CE and TSS components.

4.1 WFRA RIIC Design

SBIR and FLIR Systems/Indigo Operations embarked on the WRFA RIIC design in early 2004. The selected architecture is illustrated in Figure 5. The array features a 768 (V) x 1536 (H) configuration, and uses six onboard DACs to convert digital scene data into per-pixel analog emitter drive signals. The WFRA array features a true left-to-right raster mode, enabling sync with wide-format scanning UUTs. The WFRA RIIC also supports a static window mode, in which a 768 x 1024 region may be updated at increased frame rates.

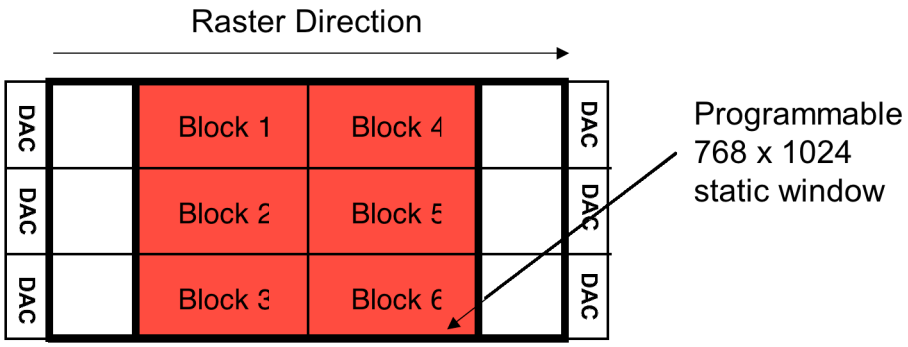


Figure 5 – WFRA RIIC Architecture

The WFRA RIIC supports both raster and snapshot frame update modes, and may be operated with independently controllable frame rate, frame update mode, and full-frame/window control. The range of supported frame rates for each window and update mode is illustrated in Figure 6.

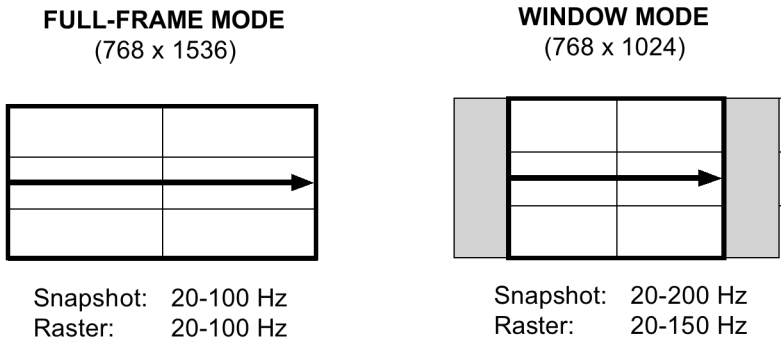


Figure 6 – WFRA Raster, Snapshot, Window, & Frame Rate Modes

As with LFRA, the WFRA RIIC includes a dedicated emitter anneal mode, reduced temporal "lag" effect, and a digital input "data clipping" function to limit the drive applied to sensitive emitter pixels. As with all of our previous RIIC designs, the WFRA device also includes a host of advanced telemetry and testability functions to ease design verification testing and system integration.

4.2 WFRA Performance

Using an emitter unit cell design very similar to that currently in fabrication on LFRA, the WFRA array is able to meet its required performance levels with a reduced level of emitter drive power, thereby minimizing total power dissipated in the DEE. Predicted WFRA radiometric performance is shown in Figure 7.

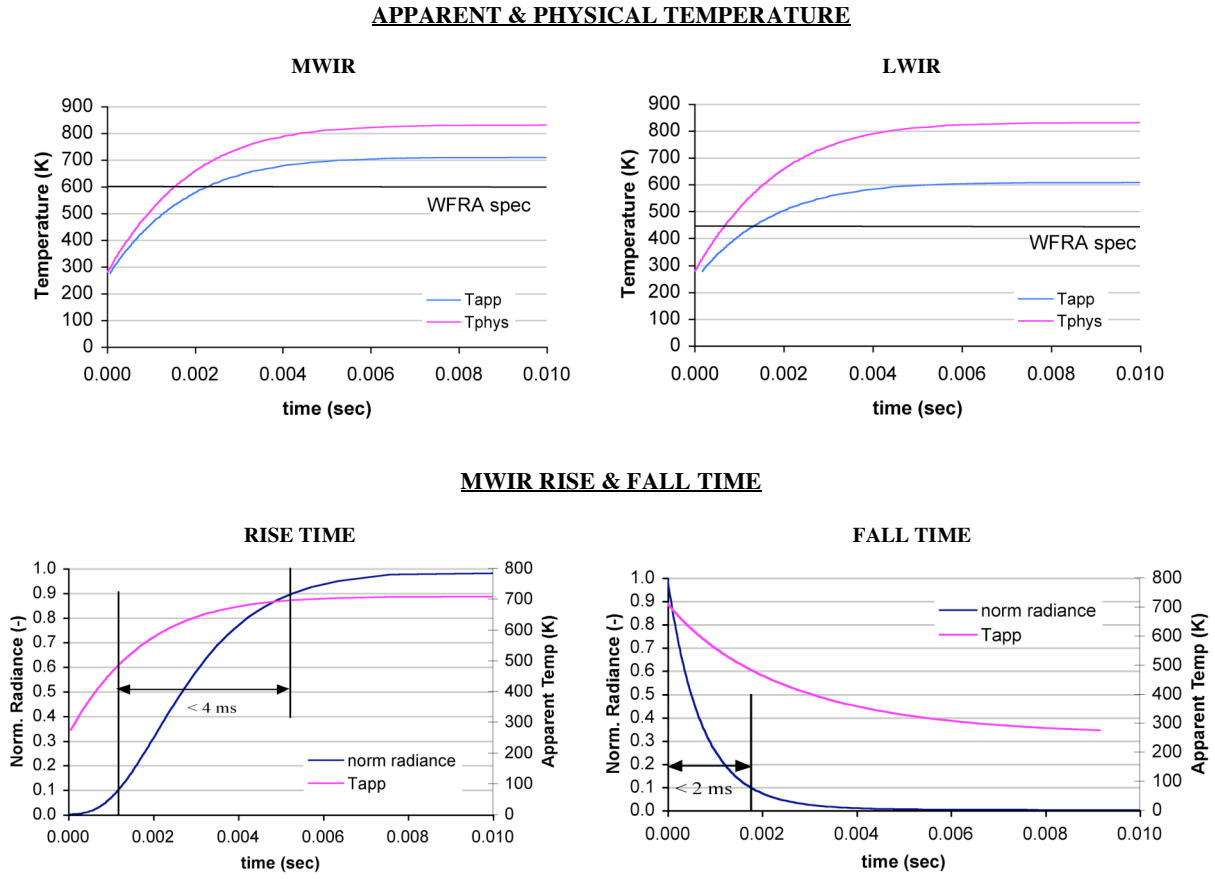


Figure 7 – Predicted WFRA Apparent/Physical Temperature & Radiance Rise/Fall Time

4.3 WFRA System Development

The WFRA C&CE will use the same fundamental hardware configuration as LFRA, including the baseline video combiner, TIP, RPP, TRP, and OPP functions. Software and firmware modifications will be made to support the unique WFRA array configuration, while maintaining the same image rotation, image flip, NUC, convolution, and other capabilities originally developed for LFRA.

5. OASIS

The Optimized Array for Space-based Infrared Simulation (OASIS) program is developing cryogenic projector array assemblies for use in cryogenic chamber-based IR scene projection. The Air Force Research Laboratory Munitions Directorate's (AFRL/MN) Kinetic Kill Vehicle Hardware-in-the-Loop Simulator (KHILS) facility at Eglin AFB has been leading the development, with SBIR responsible for design, fabrication, and development of the array and cryogenically optimized package. Array development began in 2002, with design of the 512 x 512 RIIC at Raytheon Vision Systems (RVS). The RIIC was fabricated in 2004, and wafer testing is nearing completion. Emitter pixel design and process development is complete, and emitter fabrication will start in spring 2005. Cryogenic package design is complete, with the prototype hardware build expected in mid 2005.

5.1 OASIS RIIC Performance

As reported at previous SPIE conferences, the OASIS RIIC features a selectable analog/digital scene data input interface, a low-noise signal path, a dedicated anneal mode, zero "lag effect", selectable raster/snapshot frame update, and other advanced functions and features.

OASIS presented many unique technical challenges. The array was designed to provide high apparent temperature and fast radiance rise/fall characteristics at the emitter under all operating conditions. This introduced a significant design challenge for both the RIIC and the emitter, since both CMOS and MEMS electronic and material characteristics change dramatically over the very wide operating temperature range. Particular areas of RIIC design challenge included the on-chip DAC, unit cell amplifier, low-noise analog signal path, and emitter current supply/return circuits. The RVS RIIC team overcame numerous hurdles in the design process, including substrate freeze out at cryogenic temperatures, accurate FET simulation vs. temperature, and emitter high-current supply/return routing. The OASIS RIIC uses Reticle Image Composite Lithography (RICL) to fabricate the approximately 1 x 1 inch integrated circuit. The OASIS RIIC floor plan and top-level layout are shown in Figure 8.

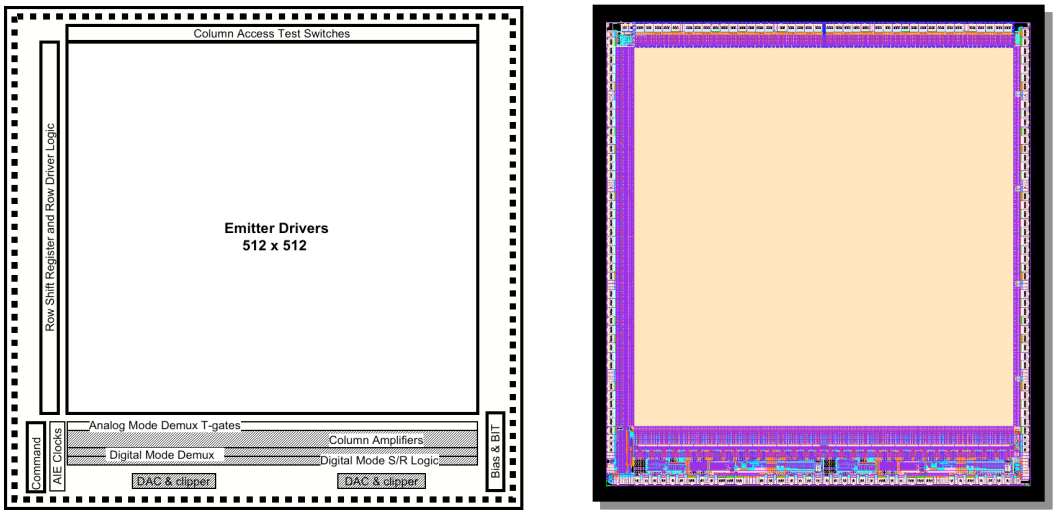


Figure 8 – OASIS RIIC Floor Plan (left) & Top-Level IC Layout (right)

OASIS RIIC wafers were fabricated at AMI in mid-2004. Wafer probe testing began in late 2004 at SBIR, using our in-house probe station and customized OASIS RIIC test software. Initial Design Validation Tests (DVTs) have confirmed

that all key functional blocks are performing as designed. As shown in Figure 9, the OASIS RIIC meets its as-designed maximum emitter drive current spec of 200 μA in normal "projection" mode, and can provide over 220 μA in "anneal" mode. Spatial uniformity of emitter drive current is excellent, as illustrated in the rightmost plot of Figure 9.

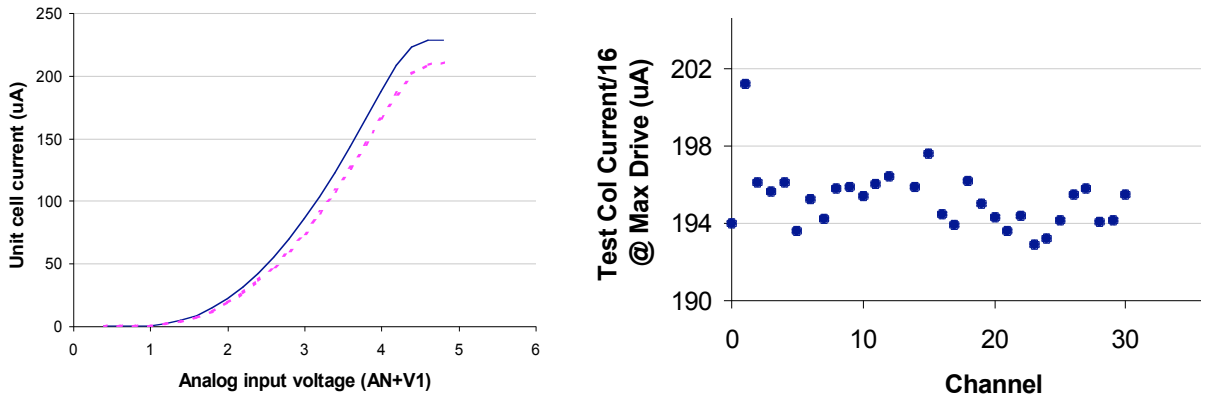


Figure 9 – OASIS RIIC Unit Cell Performance Data

The two, on-chip, 14-bit DACs function as designed, producing an output swing which slews the unit cell input current from full "OFF" (zero drive) to maximum "ON" (200 μA). For optimum DNL and INL performance, the uppermost DAC bits include calibration registers, allowing the user to optimize the DAC transfer function in the electronic domain, thereby ensuring the best possible radiometric integrity at the system level. Both raster and snapshot update modes have been verified, and we are nearing completion of all remaining DVT tests for both analog and digital input modes. Completion of lot 1 RIIC wafer screen testing is imminent, and will be followed by wafer coring, prep, and emitter processing at MCNC-RDI.

5.2 OASIS Emitter Pixel Design

In 2004, SBIR and MCNC-RDI completed the design and layout of the OASIS emitter pixel, based upon the flowdown from the OASIS IRSP specification to the RIIC and emitter levels, and the previously validated SBIR emitter performance model. The design is optimized to provide balanced temperature and rise/fall time performance margin against the OASIS specifications. The final OASIS emitter pixel layout is shown in Figure 10.

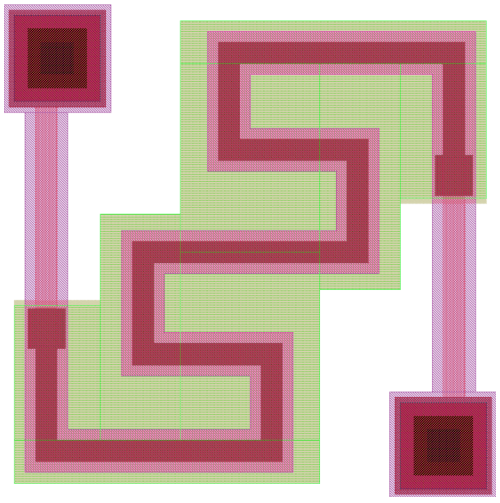
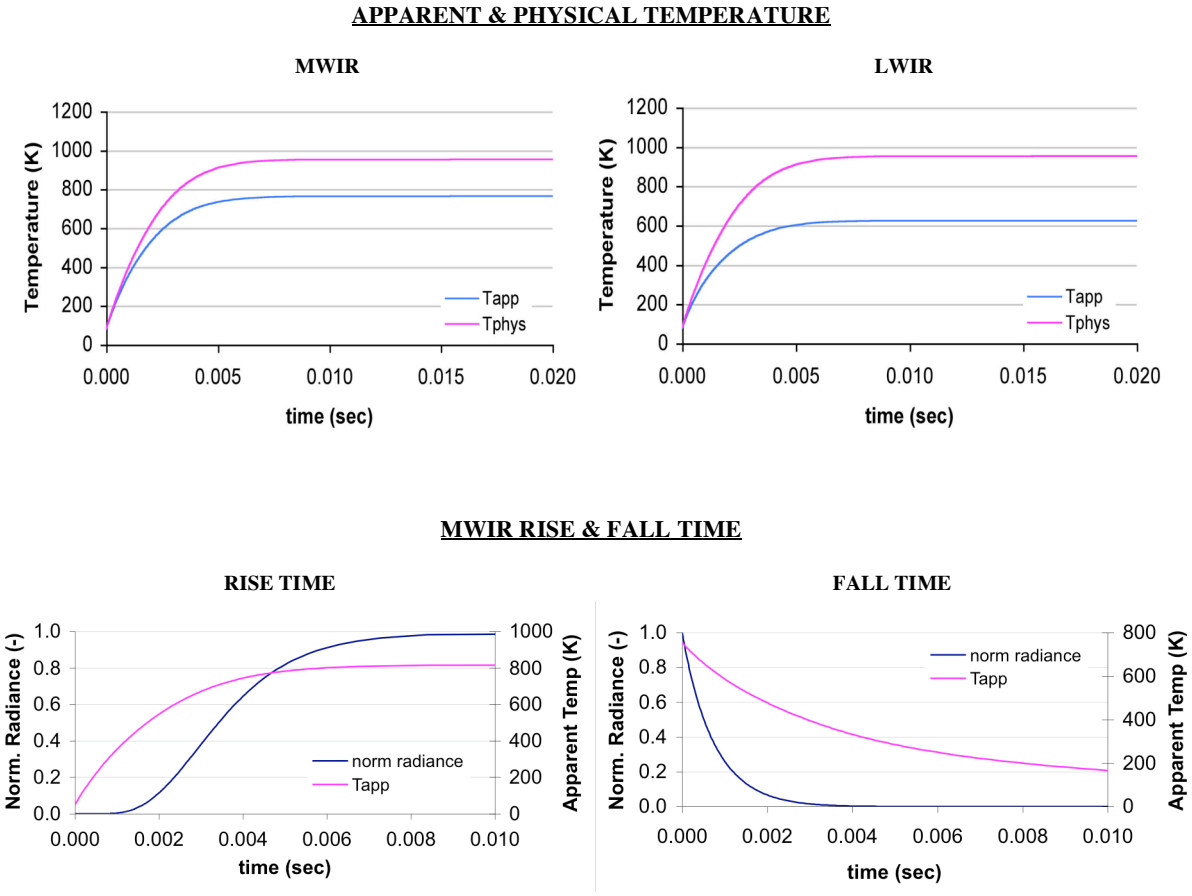


Figure 10 – OASIS Emitter Unit Cell Layout

The emitter unit cell layout has a more than 50% optical fill factor, an advanced "gossamer" bridge structure, leg geometry optimized for temperature and speed performance, and a 20 kΩ (nominal) post-anneal emitter resistance. The physical configuration of the OASIS pixel directly leverages SBIR and MCNC-RDI's experience base in designing and fabricating pixels for MIRAGE 1.5 and LFRA.

5.3 OASIS Performance

Predicted OASIS IRSP-level temperature and rise/fall time performance are summarized in Figure 11. The design exploits the temperature dependence of the emitter leg thermal conductance and emitter body heat capacity to provide extended top-end performance, even while operating at very low substrate temperatures. These predictions assume a 50 K RIIC substrate temperature, 3-5 μm and 8-12 μm IR spectral bands (MWIR and LWIR), and 95% optics/window transmission. Figure 11 summarizes the OASIS radiometric performance predictions, based upon measured RIIC characteristics and baseline emitter design parameters.



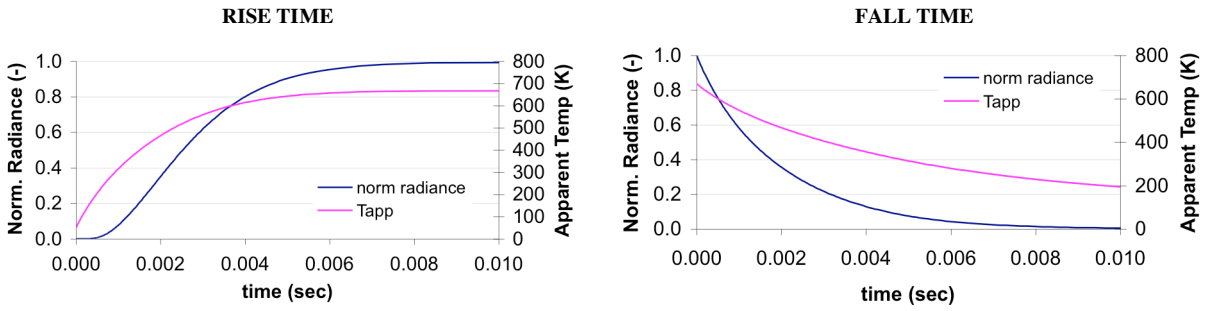


Figure 11 – Predicted OASIS Apparent/Physical Temperature & Radiance Rise/Fall Time

These performance predictions include sufficient margin to allow for significant variations in both RIIC and emitter fabrication processes, with no adverse effects in top-level projector performance after non-uniformity correction (NUC).

5.4 OASIS Cryogenic Package Design

SBIR has completed the detailed design of the OASIS cryogenic emitter package, incorporating several novel design and fabrication approaches to best support operation under both cryogenic and ambient operating conditions.

Finished emitter arrays are installed into custom ceramic packages, using proprietary bonding techniques. The ceramic package has lead frame traces for data and control I/O, four large metal buss tabs for connection of the high current emitter power supply and return leads, a window/array shield mount, and an integral vacuum feed-through. The ceramic package mounts to a proprietary meso-channel cooling plenum, which uniformly removes up to 300 W peak dissipation. The cooling plenum mounts to a large heat sink, which then installs into either the ambient test stand or the cryogenic chamber.

The OASIS cryogenic package and highly advanced ceramic chip carrier are shown in Figure 12.

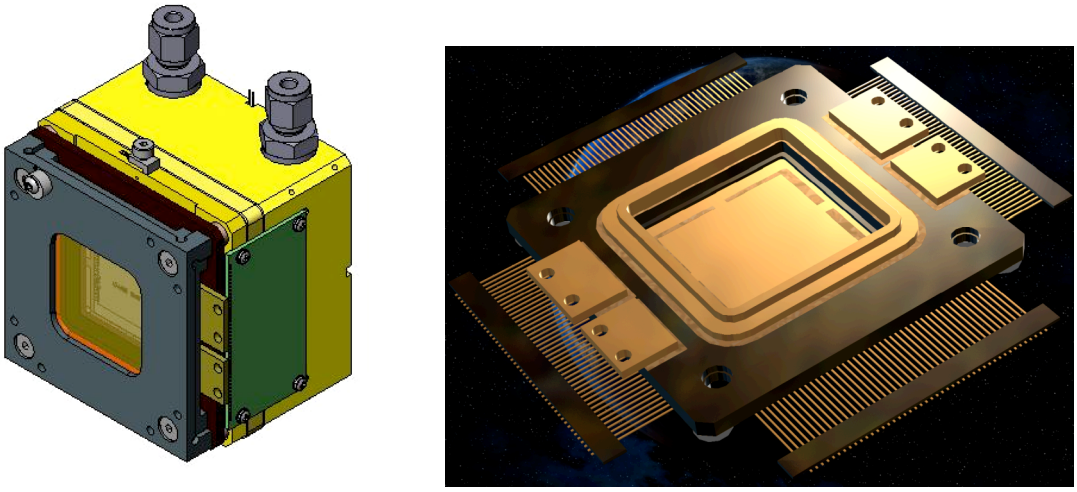


Figure 12 – OASIS Cryogenic Package (left) and Multi-Layer Ceramic (MLC) Chip Carrier (right)

The OASIS cryogenic package includes a removable, o-ring sealed window with a directly deposited thin film array shield. The window/array shield design is modular, allowing the user to install different windows for different simulation needs. The package also includes three passive electronic interface "paddleboards" and a resistive block heater, for fine-tuning the substrate temperature during operation.

5.5 OASIS System Integration

SBIR is also developing an Output Personality Processor (OPP) and Close Support Electronics (CSE) unit in support of the OASIS installation at KHILS. The OPP is a PCI card, which may be installed in a KHILS PC-Based Array Control Electronics (PACE) or SBIR "MIRAGE II" C&CE to fiber-optically drive OASIS scene data to the CSE/array. The CSE will include digital, analog, and controller boards to format and distribute scene data to the RIIC, and provide all necessary bias and timing functions required for array operation. We plan to report on system integration and OPP/CSE details at future conferences.

6. MIRAGE II

MIRAGE II, the next-generation 512 x 512 IRSP system, is also in development at SBIR. The first three systems have been delivered, with interim MIRAGE 1.5 DEEs provided until MIRAGE II DEEs start production.

6.1 MIRAGE II Array Development Status

The baseline MIRAGE II emitter array is a derivative of the LFRA design, fabricated in a 512 x 512 configuration using the same photolithographic CMOS stitching process as LFRA. The first MIRAGE II RIIC lot has completed fabrication, and is approaching wafer probe testing.

Predicted MIRAGE II performance is comparable to that of LFRA. The MIRAGE II RIIC and emitter use the same unit cell designs, and thermal/electrical IRSP system components have been sized to handle the more stressing static and dynamic loading of LFRA, and are thus easily capable of supporting MIRAGE II. The MIRAGE II RIIC has four (4) onboard DACs, as opposed to two on the original MIRAGE I device. This extra DAC parallelism allows the RIIC to update the array in half the frame time – *i.e.* at two times the frame rate – allowing finer temporal step resolution during simulation, and true 400 Hz projection when used with emitters optimized for speed. MIRAGE II will be available with multiple emitter configurations: optimized for speed, dynamic range, or balanced thermal-temporal performance. The high-speed emitter variant will allow the full-frame, 400 Hz capability of the MIRAGE II RIIC to be exploited, thereby enabling simulation of 400 Hz imagery with radiance rise/fall times of approximately 2.5 ms.

6.2 MIRAGE II Command & Control Electronics (C&CE)

Delivery of the second and third MIRAGE II C&CE systems took place in 2004. Based on the TIP/RPP/OPP architecture developed on LFRA, the MIRAGE II C&CE provides compatibility with MIRAGE 1/1.5 DEEs, and upgradeability to support LFRA, WFRA, and OASIS arrays in the future. Figure 13 shows the MIRAGE II C&CE configuration, which consists of the main C&CE rack and display/control peripherals.

Figure 13 – Production MIRAGE II Command & Control Electronics (C&CE)

The MIRAGE II C&CE will also be upgradeable to incorporate advanced processing features from LFRA, such as Translation/Rotation Processing (TRP), and convolution.

SUMMARY

SBIR is completing design of the remaining LFRA system components, and expects to begin LFRA system integration in Q2 2005. The OASIS RIIC, designed by SBIR and RVS, has completed validation testing and will be ready to support the planned start of emitter fabrication in March 2005. The OASIS cryogenic package design is complete, with prototype fabrication expected this summer. The MCNC-RDI emitter foundry has made tremendous strides in process improvement and in making the transition from "technology transfer" to "production" mode. The WFRA RIIC design has been completed by SBIR and FLIR/Indigo Operations, and is now in fabrication. Multiple MIRAGE II C&CEs have been delivered, with RIIC test, emitter fabrication, and DEE design slated to begin in late 2005. Overall, a large number of enabling technologies, qualified vendors, and novel design solutions have been brought to bear on the task of creating the most advanced IRSP systems to date. Stay tuned for the first LFRA and OASIS radiometric system performance data at next year's conference!

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