# 1024 x 1024 Large Format Resistive Array (LFRA)
# Design, Fabrication, and System Development Status

Paul Bryant, Jim Oleson, Brian Lindberg, Kevin Sparkman, Steve McHugh
Santa Barbara Infrared, Inc., 30 S. Calle Cesar Chavez, Suite D, Santa Barbara, CA 93103

Steve Solomon
Acumen Consulting, P.O. Box 6084, Santa Barbara, CA 93160

## ABSTRACT

Resistive emitter-based IRSP technology still leads the industry in terms of a flickerless, high dynamic range test solution. Santa Barbara Infrared (SBIR) is producing a high performance 1024 x 1024 Large Format Resistive emitter Array (LFRA) for use in the next generation of IR Scene Projectors (IRSPs). The CMOS Read-In Integrated Circuit (RIIC) was designed by SBIR and Indigo Systems, and fabricated at AMI Semiconductor. Performance and features include > 700 K MWIR maximum apparent temperature, 5 ms radiance rise time (10-90 %), 200 Hz full frame update, and 400 Hz window mode operation. Ten 8" CMOS wafers have been fabricated and preliminarily characterized. Emitter pixel design is underway and emitter fabrication is scheduled to start at Microelectronics Center of North Carolina Research & Development Institute (MCNC-RDI) in mid-2003. This paper discusses the RIIC design, wafer probe test results, emitter pixel design, emitter fabrication plans, packaging and test plans, and reports on 1024 x 1024 IRSP system component development status.

**Keywords:** Infrared, Scene Simulation, IR Scene Projection, 1024 x 1024 Large Format Resistive emitter Array (LFRA), CMOS, Resistive Array, IR Emitters.

## 1. INTRODUCTION

This paper describes the specification, performance, design, and fabrication of large-format, resistive, 1024 x 1024 IR scene projector (IRSP) arrays. This technology is being developed to provide improved IR scene projection capability that will keep pace with the ongoing improvements to IR detector arrays and imaging/detection systems. Unit Under Test (UUT)/imaging sensor arrays are evolving toward larger array formats, smaller pixels, and higher overall sensitivity and discrimination. IRSP systems must also continue to improve in order to support test and evaluation (T&E) of current and future sensors, trackers, and associated algorithms. This paper describes the design of 1024 x 1024 IR scene projector components, leveraging the existing SBIR MIRAGE (512 x 512) emitter array/RIIC architecture and exclusively licensed Honeywell emitter technology. This next generation resistive IRSP incorporates sophisticated architectural and design features, enabling its 2x2-inch array chip to satisfy Tri-Service performance objectives, while maximizing production yield and minimizing technical risk.

## 2. REQUIREMENTS

Projector and array-level requirements plus selected RIIC flow-down specs are summarized in Table 1. The LFRA system will produce apparent temperatures in excess of 700 K in the MWIR (3-5 μm), and greater than 500 K in the LWIR (8-12 μm). The new IRSP system is required to provide 10-90% radiance rise time of less than 5 ms, and LFRA will support this with margin, particularly in the LWIR.

| PROJECTOR ARRAY REQUIREMENTS | |
|---|---|
| Apparent Temperature (max) | > 700 K (MWIR) |
| | > 500 K (LWIR) |
| Radiance Rise Time (10-90%) | < 5 ms (MWIR) |
| | < 4.5 ms (LWIR) |
| Frame Rate | 20-200 Hz (full-frame) |
| | Up to 400 Hz (window-mode) |
| Array Configuration | 1024 x 1024 |
| Unit Cell Size | 48 x 48 μm |
| Frame Update Modes | Snapshot, Raster |
| Windowing | 512 x 1024, static |

| RIIC FLOW-DOWN REQUIREMENTS | |
|---|---|
| Emitter Drive Mode | Current |
| Emitter Resistance (nom) | 20 kΩ |
| Emitter Drive Power | 700 μW (spec) |
| | 800 μW (goal) |
| Drive Resolution | > 14-bit effective |
| Anneal Mode Headroom | > 10 % (power) |

**Table 1 – LFRA Specifications & Flow-Down Requirements**

The array operates at frame rates between 20 Hz and 200 Hz in normal 1024 x 1024 mode (full-frame), and at frame rates up to 400 Hz in 512 x 1024 static window mode.

## 3. RIIC DESIGN & FABRICATION

The 2 x 2-inch LFRA RIIC architecture is shown in Figure 1. The core is partitioned into eight 256 x 512 regions, each served by a dedicated digital-to-analog converter (DAC) stage.

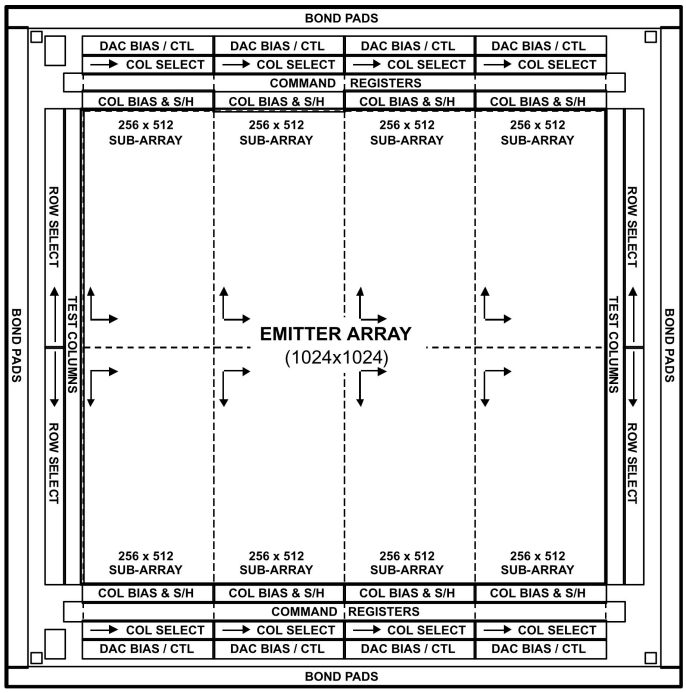


**Figure 1 – LFRA RIIC/Emitter Array Floor Plan**

The LFRA array offers a number of advanced features including support of both snapshot-mode and raster-mode frame update for flexible synchronization compatibility with both staring and scanning UUTs. For high frame rate UUTs, varying horizontal/vertical aspect ratios, and special UUT algorithm development, the LFRA array supports a 512 x 1024 static window mode. In this mode, fully programmable 512 x 1024 scene content may be provided to the projector, at frame update rates up to 400 Hz. In window mode, the top and bottom periphery regions are driven to separate and non-time-varying background levels – thereby providing pseudo-full-frame imagery with static "land/sky" content, at rates up to 400 Hz.

Each of the eight on-chip DACs has programmable offset and LSB/MSB step size in order to maximize projector dynamic range, minimize NUC complexity, and optimize system performance. This programmability is provided via the digital interface, and includes sufficient range to compensate for non-uniformities and mismatches that result from RIIC and emitter pixel process variations.

In order to provide greater than 700 K MWIR apparent temperature and less than 5 ms radiance rise time, very high pixel power levels are required – 700 μW, minimum. The need to deliver these emitter pixel power levels independent of substrate and buss effects forced the design to a current-mode emitter drive scheme.

The array also provides a dedicated "anneal mode", allowing pixels to be driven to annealing temperatures prior to system integration, and then locked out from achieving such temperatures during normal projection. In anneal mode, the RIIC transfer function is altered such that commanding maximum drive results in approximately 1 mW of pixel power, as illustrated in figure 2.

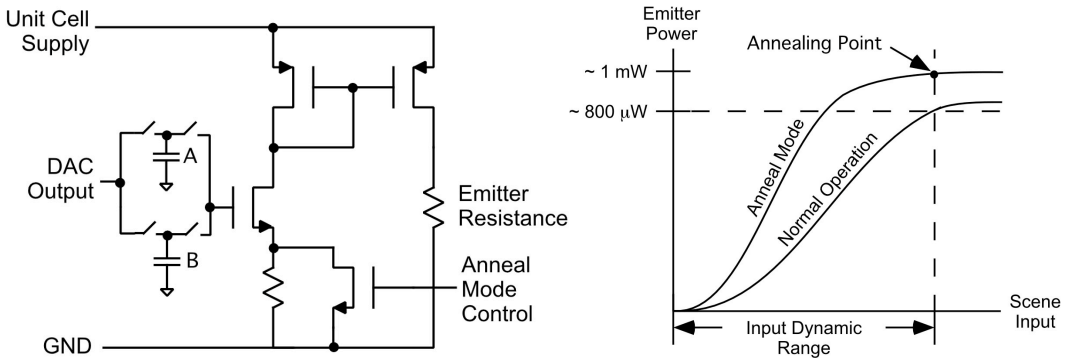


**Figure 2 – LFRA Unit Cell Topology (left) and Projection/Anneal Mode Transfer Functions (right)**

Due to saturation effects in the unit cell current mirror stage, excitation of a sparse grid of pixels using this approach will not only result in high temperature annealing, but also a very uniform spatial distribution of anneal temperature. Post-anneal non-uniformity will then be limited only by emitter resistance and RIIC drive current variations, and overall array performance will be improved.

The LFRA RIIC was fabricated at AMI Semiconductor, using a state-of-the-art 8-inch CMOS processing line. The wafers have two layers of polysilicon, five layers of metal, and are patterned using a "stitched" technique, which allows precision photolithography of very large devices. Finished LFRA wafers are shown in figure 3.

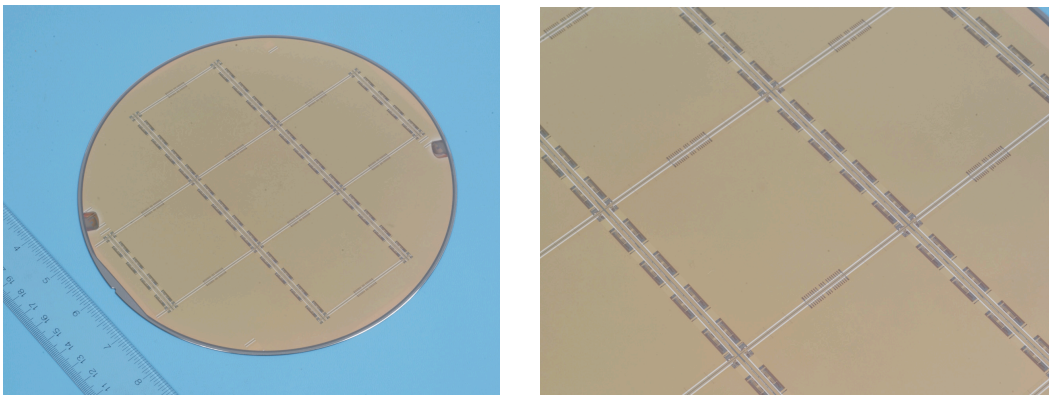

**Figure 3 – Completed LFRA RIIC Wafer (left), Close-Up (right)**

As figure 3 shows, the LFRA wafer contains 5 complete RIIC dice. Wafer probing is accomplished using SBIR's new probe station. A linear array of probe tips connects to one side of a RIIC die at a time, applies all bias and timing functions, and brings out test point signals to a rack of measurement electronics. In this way, each RIIC is probed in "half chip" steps, which is well suited to the LFRA device since the array is separated into electrically-independent top and bottom halves by design.

## 4. RIIC PROBE TEST DATA

LFRA RIIC wafer probing activities have so far been focused on design validation and evaluation of key circuit blocks. Based upon four wafers measured to date, we have verified that the on-chip DACs, digital logic blocks, serial command interface, shift registers, temperature sensors, and test/diagnostic modes are functional. Automated unit cell continuity testing (ie, array operability mapping) will be online shortly.

In addition to DAC coarse functionality, such parameters as adjustment capability, MSB output range, output offset, bias current, and test modes have been verified. Direct and buffered DAC output test points have been used to measure performance. DAC yield is approximately 50%, based upon data from the first four wafers tested. Figure 4a shows the measured output curve for a typical LFRA on-chip DAC. This data correlates well with simulation results from the design phase.

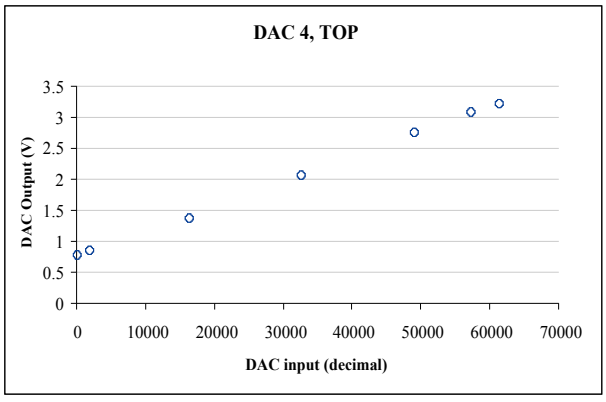


**Figure 4a – DAC Output Voltage vs. Input Data Word**

In order to maximize raw array uniformity, the LFRA DAC MSB/LSB step size and output offset parameters are adjustable via the RIIC's serial command data interface. Figures 4b and 4c illustrate the adjustability of DAC output at maximum drive (4b) and DAC output offset at zero input drive (4c).

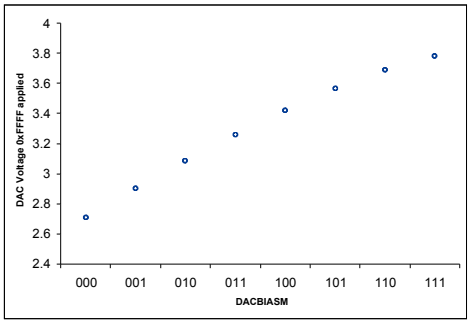


**Figure 4b – DAC Range vs. MSB Bias Adjustment**

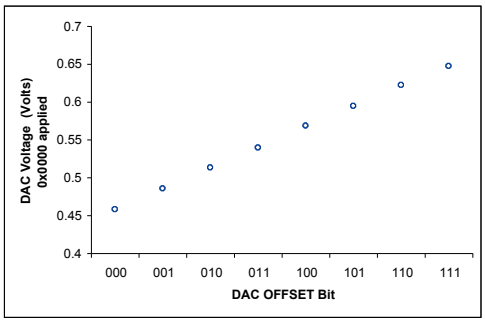


**Figure 4c – DAC Output vs. Offset Adjustment**

Wafer probing will continue into summer 2003, with the goal of completely characterizing all wafers and selecting candidate devices for emitter fabrication.

## 5. EMITTER ARRAY PERFORMANCE PREDICTIONS

Based upon the measured performance of the LFRA RIIC, radiometric performance predictions for the LFRA array (RIIC + emitters), is shown in figures 5a and 5b. The predictions assume 700 μW emitter pixel power dissipation, substrate temperature of 273 K, MWIR 3-5 μm bandpass, optical window transmission of 0.95, and pixel fill factor of 50 %. All LFRA modeling uses electrical-thermal-radiometric simulation tools validated against legacy IRSP arrays.

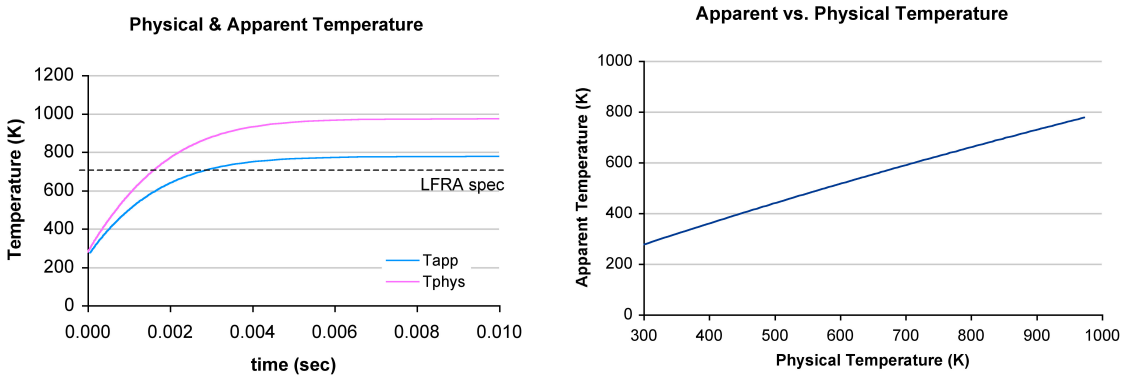


**Figure 5a – Predicted LFRA Physical and Apparent Temperature**

Figure 5b shows the predicted radiance rise time (10-90%) and fall time (90-10%) characteristics for the LFRA array. Conservative flow-down of specifications from the IRSP to both RIIC and emitter levels has resulted in moderate predicted performance margin against the specified 5 ms maximum rise/fall times.

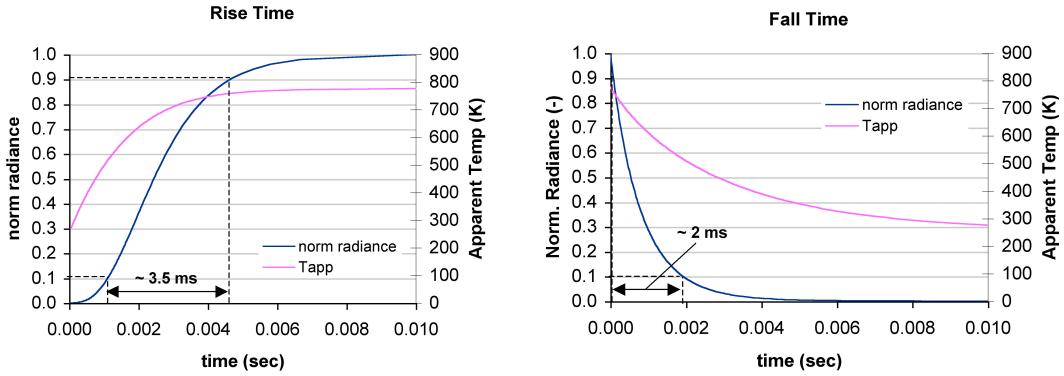


**Figure 5b – Predicted LFRA Radiance Rise & Fall Time Characteristics**

These performance predictions will be validated in late 2003 when emitter array fabrication is scheduled to be complete at MCNC-RDI, and packaging/test commences at SBIR.

## 6. EMITTER PIXEL DESIGN & FABRICATION

LFRA emitter pixel design will be a collaborative effort between SBIR and MCNC-RDI, and will leverage the success of both legacy and SBIR MIRAGE 1.5 designs. Radiometric performance of the pixel will be driven by design factors such as pixel pitch, fill factor, leg length, base resistance, dielectric thickness, and material selections. The baseline LFRA pixel design parameters are shown in table 2.

| | |
|---|---|
| Pixel Pitch | 48 x 48 □m |
| Emitter Resistance (nom) | 20 k□ |
| Optical Fill Factor | 50 % |
| Architecture | "Gossamer" |

**Table 2 – Summary of Key LFRA Emitter Pixel Design Parameters**

Detailed pixel layout and mask generation will leverage MCNC-RDI's well-proven history of successful MEMS and MOEMS designs.

Emitter fabrication will also take place at MCNC-RDI, using the same MEMS processing line used to successfully complete both material development and prototype lot activities over the last year. Prototype device performance is described in other 2003 Aerosense papers.

## 7. LFRA SYSTEM COMPONENTS

Several key LFRA system development activities are underway, including the command and control electronics, digital emitter engine, and thermal support subsystem.

### 7.1 Command & Control Electronics (C&CE)

The C&CE receives data from the scene generation platform, performs real-time non-uniformity correction (NUC) and data processing functions, and streams fiber-optic digital data and timing signals to the DEE. The LFRA C&CE is a standard PCI-based unit incorporating a single-board computer/host for control/GUI use, and a variety of input, processing, output, communications, and peripheral cards as shown in figure 6.

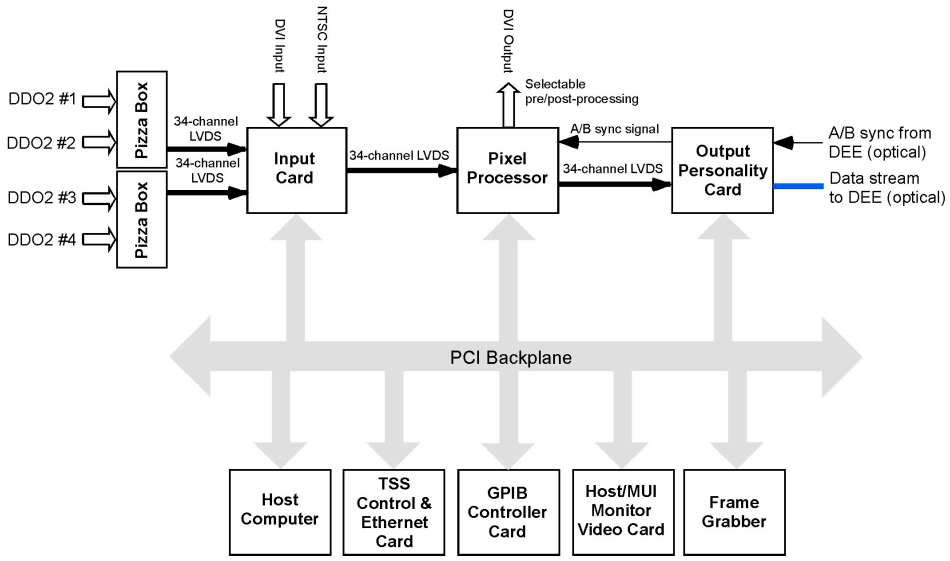


**Figure 6 – LFRA C&CE Block Diagram**

Scene data is transmitted in DDO2/DVP2 format via PECL-to-LVDS "pizza box" converters, or in DVI format directly to the Timing & Input Processor (TIP) card. Shown in figure 7a, the TIP also accepts NTSC input, serves as internal clock/sync master for the C&CE, and routes data into the Reconfigurable Pixel Processor (RPP) card. The RPP (figure 7b) performs image flip, real-time NUC using up to 16 breakpoints, with a variety of other DSP functions such as image rotation, overdrive/underdrive, convolution, and buss bar robbing compensation under development. The C&CE architecture is scalable, and RPP cards may be cascaded to increase DSP capability as real-time functions are developed in the future. Both TIP and RPP designs have been developed by Eglin AFB/KHILS under the PC-Based Array Control Electronics (PACE) and LFRA programs, and have been successfully demonstrated.

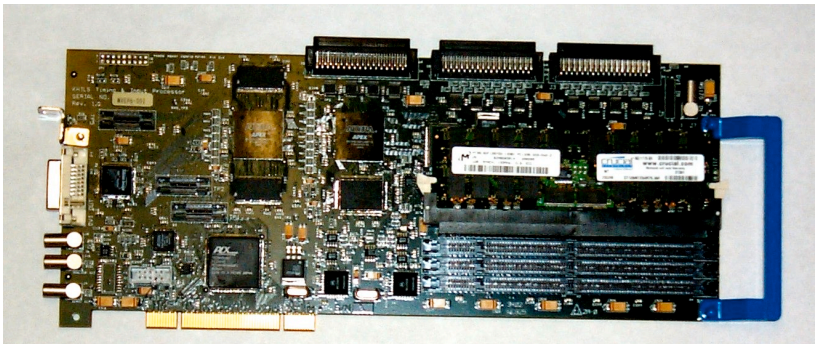

**Figure 7a – LFRA Timing & Input Processor (TIP) Card**

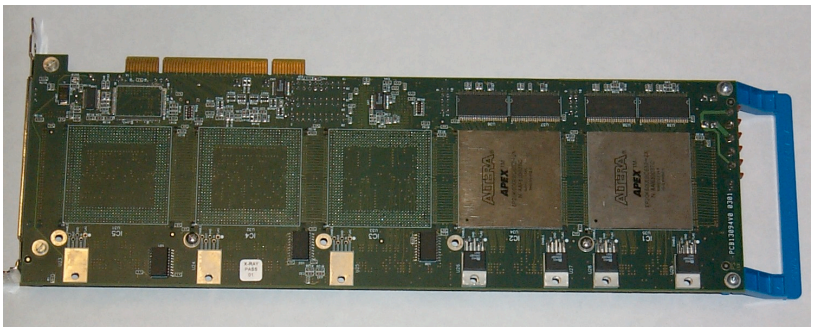

**Figure 7b – LFRA Reprogrammable Pixel Processor (RPP) Card**

The first of the SBIR-designed output personality cards is the MIRAGE 1/1.5 ("M1") PCI board. The M1 output board, shown in figure 7c, receives data from the RPP, performs DAC linearization, and transmits optical digital data to a first-generation MIRAGE 1/1.5 DEE at up to 200 Hz. The board has been designed to support all MIRAGE systems, as well as provide the ability to validate the LFRA C&CE design using an existing MIRAGE dewar – well in advance of LFRA dewar availability. The M1 output board has been successfully integrated with a MIRAGE 1 DEE, thereby validating the hardware and firmware design.

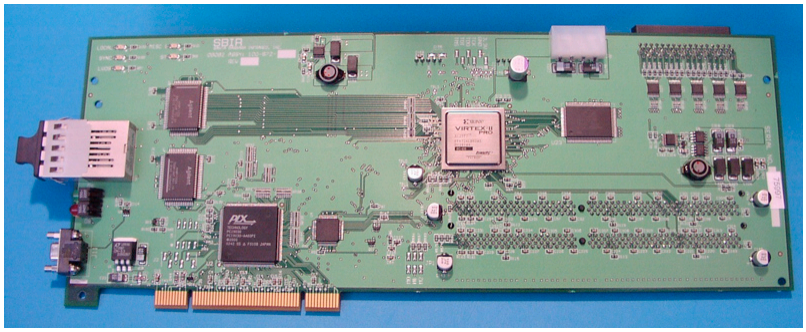

**Figure 7c – MIRAGE 1/1.5 Output Card for LFRA C&CE Checkout**

The M1 output board has been designed and configured for expandability to the LFRA configuration. Like the core TIP and RPP PACE components, the SBIR output board is a PCI device designed around an FPGA, incorporating onboard LUT and simulation memory, and offering the advantage of flexible re-programmability via the PCI bus. The optical transceiver used in the MIRAGE 1/1.5 output board is backward compatible with all MIRAGE 1 DEEs. For LFRA, MIRAGE II, and other upcoming configurations, the Agilent fiber-optic serializer/deserializer chipset will be upgraded to a XENPAK 10 Gigabit optical transceiver to improve bandwidth and simplify design integration.

### 7.2 Digital Emitter Engine (DEE)

LFRA DEE thermal design is crucial due to the fact that the array dissipates high "typical" and "peak" power levels - 500 W for typical, 1000 W peak. To minimize array heating and scene-dependent thermal crosstalk effects, the DEE/dewar is being designed to include:

- An extremely robust solder joint between RIIC and fanout board,
- Low thermal impedance from fanout board to heat sink, and
- A large heat sink for maximum thermal mass and conductance.

An optimized solder re-flow die attachment process is under development, minimizing voids and other issues which can limit thermal performance due to localized array heating and/or thermal background gradients on the order of tens of Kelvins.

The DEE is being designed for very low impedance on high-current emitter power supply and return lines – less than 0.1 m series resistance and 5 nH inductance. Extensive complementary supply bypassing will be implemented on a hybrid fanout board utilizing BeO and PCB materials, and numerous high and low frequency filter banks will be located in proximity to the emitter array itself. Several novel "constant current DEE" implementations are being evaluated to minimize scene-dependent electrical transients.

### 7.3 Thermal Support Subsystem (TSS)

In LFRA TSS configuration, a high-capacity chiller will handle LFRA's high static and dynamic thermal loads. One or more high-current power supplies will provide 100-200 A, as drawn by the DEE under typical and worst-case IRSP scenarios.

Due to the high electrical and thermal loading of the LFRA IRSP, multiple levels of hardware and software interlock are being implemented to protect sensitive system components and avoid accidental emitter re-annealing or damage.

## 8. SUMMARY

Development of the LFRA system and key subcomponents is proceeding rapidly. The first RIIC devices have been fabricated, and design verification testing is in progress. Results to date are positive, and testing is expected to be completed in mid-2003, in anticipation of an emitter fabrication start in late 2003. Development of C&CE, DEE, and TSS components are underway, with prototype C&CE hardware successfully demonstrated.

## ACKNOWLEDGMENTS

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