1,024 x 1,024 Resistive Emitter Array Design & Fabrication Status

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ABSTRACT

Santa Barbara Infrared (SBIR) is producing a high performance 1,024 x 1,024 Large Format Resistive emitter Array (LFRA) for use in the next generation of IR Scene Projectors (IRSPs). LFRA requirements were developed through close cooperation with the Tri-Service IR Scene Projector working group, and through detailed trade studies sponsored by the OSD Central T&E Investment Program (CTEIP) and a Phase I US Navy Small Business Innovative Research (SBIR) contract. The CMOS Read-In Integrated Circuit (RIIC) is being designed by SBIR and Indigo Systems under a Small Business Innovative Research (SBIR) contract. Performance and features include 750 K MWIR maximum apparent temperature, 5 ms (10-90 %) radiance rise time, 200 Hz full frame update, and 400 Hz window mode operation. Ten 8" CMOS wafers will be fabricated and characterized in mid-2002, followed by emitter fabrication in late 2002. This paper discusses array performance, requirements flow-down, array design, fabrication of 2 x 2-inch CMOS devices, and plans for subsequent RIIC wafer test and emitter pixel fabrication.

Keywords: Infrared, Scene Simulation, IR Scene Projection, 1,024 x 1,024 Large Format Resistive emitter Array (LFRA), CMOS, Resistive Array, IR Emitters.

1 INTRODUCTION

This paper describes the specification, performance, design, and fabrication of large-format, 1,024 x 1,024 IR scene projector (IRSP) arrays. This technology is being developed to provide improved IR scene projection capability that will keep pace with the ongoing improvements to IR detector arrays and imaging/detection systems. Unit Under Test (UUT)/imaging sensor arrays are evolving toward larger array formats, smaller pixels, and higher overall sensitivity and discrimination. IRSP systems must therefore also evolve along commensurate paths of technological growth, in order to support test and evaluation (T&E) of current and future sensors, trackers, and associated algorithms. This paper describes the design approach being implemented toward development of a 1,024 x 1,024 IR scene projector format, leveraging the existing MIRAGE (512 x 512) emitter array/RIIC architecture. This next generation IRSP will also incorporate numerous architectural and design/layout improvements enabling its 2 x 2-inch array chip to satisfy Tri-Service performance objectives, while maximizing production yield and minimizing technical risk.

2 LFRA REQUIREMENTS

Current Army, Navy, and Air Force IRSPs do not have the necessary resolution to adequately test existing and advanced sensor systems (i.e - IR sensors with imaging formats of 512 x 512, 640 x 480, 480 x 1,280, 1,024 x 1,024, and larger). Projection formats of up to 1,024 x 2,048 emitting pixels are required to cost-effectively test the next generation of IR sensor systems in the confines of the laboratory, depot, hangar, and dock. The 1,024 x 2,048 format is also required to properly support "along the horizon" racetrack search patterns for testing ship self defense, and airborne surveillance, systems. Expansion and transition of current mature resistive-emitter array technologies to large format resistive-emitter array (LFRA) full field of view (F-FOV) IR projector systems in DoD test facilities will enable full test support of the next generation of IR/EO sensor systems.

A Tri-Service sponsored array architecture study has been performed, based on the extension of Santa Barbara Infrared's MIRAGE (Multi-spectral IR Animation Generation Equipment) and Honeywell's existing emitter technology base. The study defined an expansion of MIRAGE and Honeywell's 512 x 512 emitter-array architecture to 1,024 x 1,024 and 1,024 x 2,048 emitter-array configurations. Development of the large format emitter array will involve the scaling-up of functions and features originally implemented on MIRAGE and the integration of additional features required and desired by the Government. Under this architecture development study, SBIR and Indigo analyzed the Government IRSP Test and Evaluation (T&E) requirements and developed a specification for the large format Read-In Integrated Circuit (RIIC) design. MIRAGE capabilities recommended for incorporation into the LFRA, are snapshot mode, on-chip digital-to-analog (D/A) converters, and high frame rate operation.

The key LFRA requirements provided by the Tri-Services IRSP working group, plus selected RIIC flow-down specs are summarized in Table 1. In order to satisfy all MWIR maximum apparent temperature goals, with margin, the LFRA is specified to produce apparent temperatures in excess of 700 K in the MWIR (3-5 μm), and greater than 600 K in the LWIR (8-12 μm). Radiance rise time (10-90 %) is specified to be less than 5 ms, and the LFRA will support this with margin, particularly in the LWIR. The array must operate at frame rates between 20 Hz and 200 Hz in normal 1,024 x 1,024 mode (full-frame), and at frame rates up to 400 Hz in window mode.

PROJECTOR ARRAY REQUIREMENTS	
Apparent Temperature (max)	> 750 K (MWIR)
	> 600 K (LWIR)
Radiance Rise Time	< 5 ms (MWIR)
	< 4.5 ms (LWIR)
Frame Rate	20-200 Hz (full-frame)
	Up to 400 Hz (window-mode)
Array Configuration	1,024 x 1,024
Unit Cell Size	< 50 x 50 μm
Frame Update Modes	Snapshot, Raster
Windowing	512 x 1,024, static

RIIC FLOW-DOWN REQUIREMENTS	
Emitter Drive Mode	Current
Emitter Resistance (nom)	20 kΩ
Emitter Drive Power	700 μW (spec)
	800 μW (goal)
Drive Resolution	> 14-bit effective
Anneal Mode Headroom	> 10 % (power)

Table 1 – LFRA Specifications & Flow-Down Requirements

It was realized during the specification flow-down process that in order to support the apparent temperature and radiance rise time requirements placed upon the final LFRA projector array, the RIIC needs to deliver extraordinary levels of pixel power drive, and deliver that power independent of any power buss or substrate effects. The RIIC's delivery of emitter pixel power in the 700-800 μW range is necessary in order to support LFRA speed and power requirements at the scene projector level. To achieve these levels, a current-mode unit cell drive scheme was selected. Cell pitch of less than 50 x 50 μm was selected in order to permit flexible emitter pixel design (fill factor, pixel mass, etc), while providing enough available silicon real estate to implement the unit cell circuitry required to satisfy performance objectives. Operationally, the RIIC supports the LFRA requirements for frame rate, frame update mode, windowing, annealing, adjustability, and test modes – while providing greater than 14-bit effective (16-bit input) temperature resolution, and compatibility with a variety of future emitter pixel design and layout approaches.

3 LFRA RIIC ARCHITECTURE

The very large, 2 x 2-inch LFRA RIIC architecture is shown in Figure 1. The core is partitioned into eight 256 x 512 regions, each served by a dedicated digital-to-analog converter (DAC) stage.

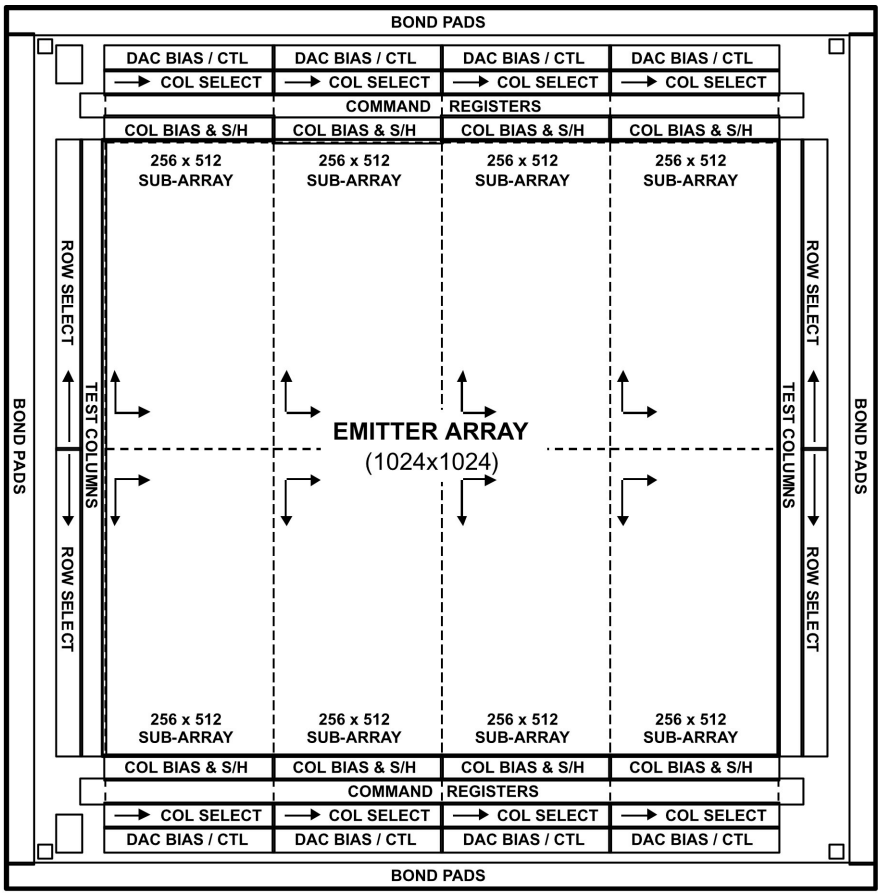

Figure 1 – LFRA RIIC Floorplan

The left and right sides of the array are populated with a large number of unit cell electrical power supply pads, in order to minimize power supply variation as a function of dynamic scene content. All other clock, bias, and digital input data functions reach the LFRA RIIC via the top and bottom edges of the chip.

3.1 EXTENDED DYNAMIC RANGE

As mentioned previously, the LFRA apparent temperature and radiance rise time requirements demand state-of-the-art power delivery to each emitter pixel. Figure 2 shows a historical sampling of performance trend-line data from both MIRAGE and other IR scene projectors. The LFRA RIIC specification and goal power levels have been the impetus for us to move into previously uncharted territory in terms of the temperature vs. speed trade-off for IR scene projection.

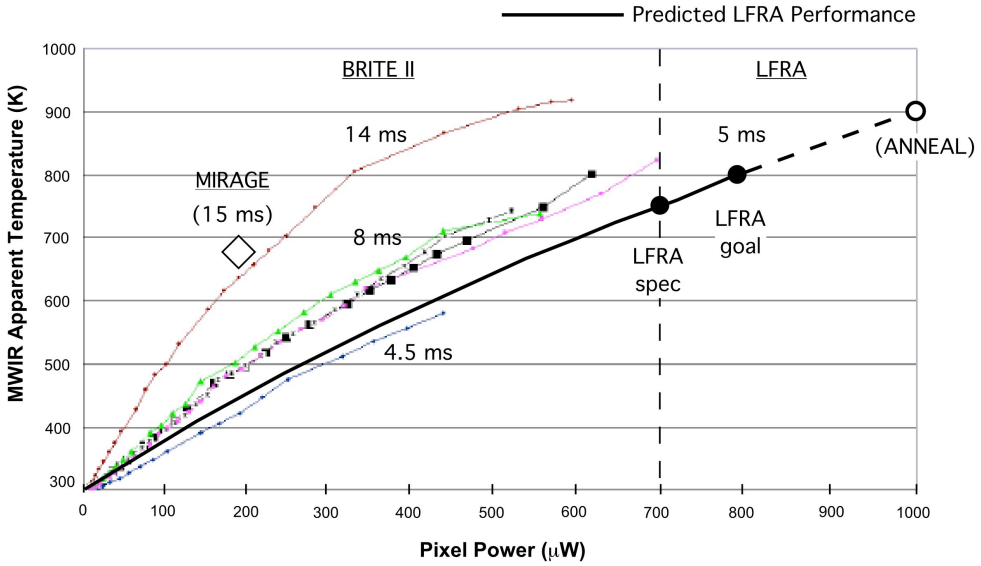

Figure 2 – LFRA Performance Trend Line

It is noteworthy that the extended dynamic range of the LFRA unit cell provides not only a unique combination of apparent temperature and radiance rise time, but also greatly decreased sensitivity to RIIC and emitter process variations. Stated differently, the performance headroom inherent in the LFRA RIIC enables more combinations of "as-fabricated" RIIC and emitter devices to yield projector arrays with spec-compliant maximum temperature and radiance rise time performance.

3.2 SNAPSHOT AND RASTER-MODE UPDATE

The LFRA array will support both snapshot-mode and raster-mode frame update. Snapshot mode is optimal for scene projection onto UUTs with large 2-D staring arrays, typically employing snaphot integration within the focal plane array. Raster mode provides improved synchronization compatibility with scanning UUTs, by more closely matching each emitter pixel's radiance rise characteristic with each detector pixel's integration window. Selection of frame update is mode is via the LFRA array's serial digital command function.

3.3 512 x 1,024 WINDOW MODE

In order to support high frame rate UUTs, varying horizontal/vertical aspect ratios, and/or special UUT algorithm development, the LFRA array supports a 512 x 1,024 static window mode. In this mode, fully programmable 512 x 1,024 scene content may be provided to the projector, with frame update rates up to 400 Hz. In window mode, the top and bottom periphery regions are driven to separate and non-time-varying background levels – thereby providing pseudo-full-frame imagery with static "land/sky" content, at rates up to 400 Hz.

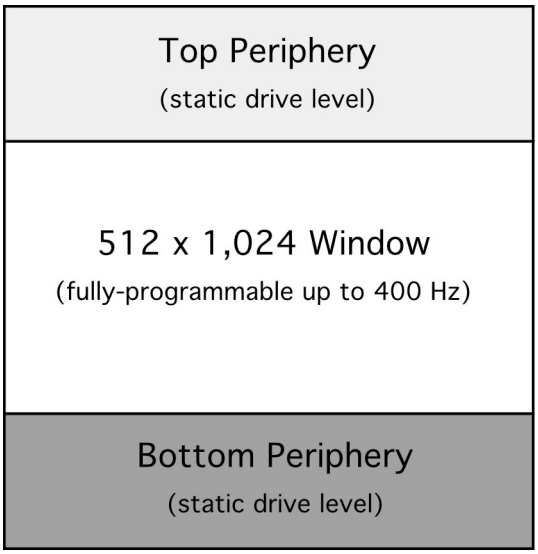

Figure 3 – 512 x 1,024 Window Mode

Figure 3 illustrates the spatial orientation of the 512 x 1,024 window, and land/sky peripheral regions. It is worth noting that for ease of electrical interfacing, the LFRA RIIC may be provided input data at a single rate to support both full-frame (1,024 x 1,024) projection at 200 Hz, and window mode (512x 1,024) projection at 400 Hz.

3.4 ANNEAL MODE

One of the key methods of attaining high-performance, stable emitter arrays is the emitter anneal process. This consists of operating pixels at very high temperatures, for relatively short durations, for the purpose of "burn-in". Future operation of the array is limited to lower physical temperatures, such that the chemical and material processes invoked during anneal are not continued during normal operation. The LFRA RIIC incorporates a mode in which over 10 % added, spatially uniform power can be delivered to the emitters for annealing purposes.

3.5 ON-CHIP, FULLY-ADJUSTABLE DACs

Each of the eight DACs on the RIIC has programmable offset and LSB/MSB step size, in order to maximize projector dynamic range, minimize NUC complexity, and optimize system performance. This programmability is provided via the digital interface, and includes sufficient range to compensate for non-uniformities and mismatches that result from RIIC and emitter pixel process variations.

3.6 PROGRAMMABLE DIGITAL INTERFACE

As mentioned previously, the LFRA array's programmable digital interface provides external control over operating mode (frame update, window, anneal, test), DAC adjustment, emitter maximum drive protection level, and other functions. Control data may be loaded periodically, as operating conditions are modified during a test sequence, or continually updated.

4 LFRA UNIT CELL DESIGN

The unit cell buffer amplifier topology is depicted in figure 4a. Dual input sample-and-hold capacitors are employed to minimize charge sharing at the input node, and dramatically reduce the frame-to-frame cross talk or, "lag" effect observed in other systems.

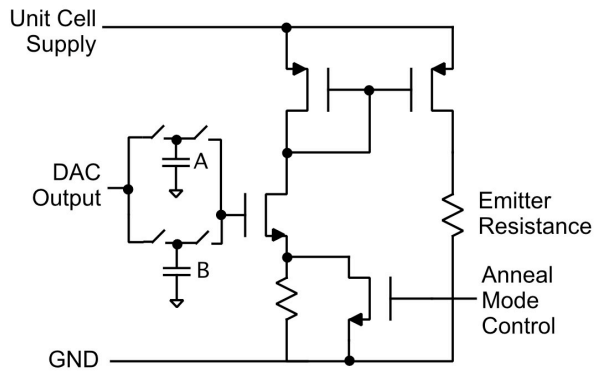

Figure 4a –
Unit Cell Amplifier Topology

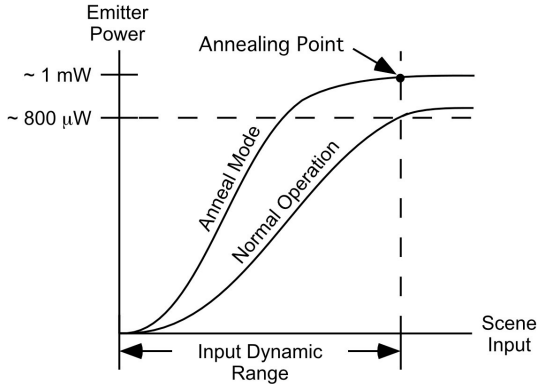

Figure 4b –
Unit Cell Transfer Function

The emitter power delivered by the current mirror with input FET source degeneration is spread over a wide range of DAC output voltage, and is more linear across the full dynamic range than more traditional topologies. Though the highly non-linear power-to-radiance transfer function of the emitter precludes the need for maximum RIIC linearity, the improved LFRA unit cell improves apparent temperature resolution without the need for very small DAC LSB voltages. Figure 4b illustrates a simplified unit cell transfer function, with depiction of the "anneal mode" characteristic invoked to deliver highly uniform, elevated power levels to the emitters for annealing purposes.

4.1 EXTENDED UNIT CELL DYNAMIC RANGE

In order to provide 750 K, 5 ms performance, very high pixel power levels are required. The need to deliver 700-800 μW per pixel, independent of substrate and buss effects, forced the design to a current-mode emitter drive scheme – as shown above. To achieve these power levels, over 200 μA of per-pixel drive current is required. RIIC performance model predictions indicate that we will achieve the required emitter power levels with margin.

When operated in "anneal mode", the RIIC transfer function is altered such that commanding maximum drive results in approximately 1 mW of pixel power. Due to saturation effects in the unit cell current mirror stage, excitation of a sparse grid of pixels using this approach will result in not only high temperature annealing, but also a very uniform spatial distribution of anneal temperature. Post-anneal non-uniformity will then be dominated by emitter resistance and RIIC drive current variations, rather than "annealed-in" fixed-pattern artifacts.

1.2 DUAL SAMPLE-AND-HOLD

The dual ("ping-pong") sample-and-hold stage at the unit cell input provides dramatically reduced frame-to-frame cross talk, by reducing the amount of charge shared between one frame and the next in snapshot mode. The dual sample-and-hold timing is synchronized with the external drive electronics, such that dual (odd/even frame) NUC tables may be used to eliminate possible effects caused unit cell capacitor mismatch.

1.3 LOW SUBSTRATE RESISTANCE

The current delivered to each emitter pixel is returned via the RIIC substrate, to minimize ground impedance across the array. As such, it is highly desirable to minimize the substrate resistance. The per-cell substrate resistance of the LFRA array will be more than 25 % lower than for the MIRAGE 512 x 512 array. Combined with the increased drive power and higher buss metallization fill factor of the LFRA design, this reduction in substrate impedance serves to maximize emitter array performance.

5 RIIC WAFER FABRICATION

Due to the RIIC's approximately 2-inch x 2-inch diced array size, conventional IC fabrication schemes and photolithographic techniques do not support production of the LFRA device. Stepped-reticle, or "stitched" fabrication will be performed in order to expose all portions of the wafer with the necessary patterns. An illustration of the stitched fabrication approach is shown in figure 5.

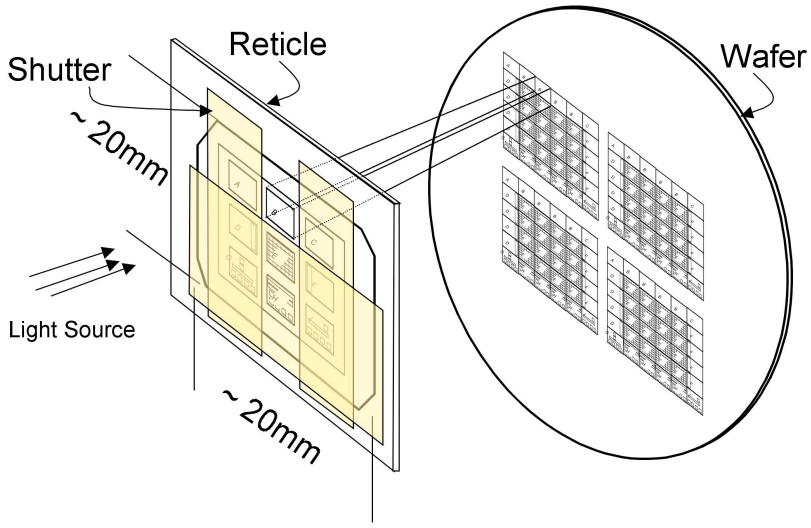

Figure 5 – CMOS RIIC Stitching Approach

Stitching has been demonstrated previously in the fabrication process selected for LFRA production. Aside from fabrication of very large integrated circuits, stepped-reticle fabrication offers the advantage of supporting "scaled" configurations, such as future 1,024 x 2,048 arrays, as well as new 512 x 512, 256 x 256, and other formats.

6 EMITTER FABRICATION & RIIC TEST PLANS

LFRA RIIC wafers will be probe tested at SBIR and will undergo a full range of validation and per-array acceptance tests. Measurements will include full characterization of onboard DAC performance, unit cell drive dynamic range, unit cell continuity, and evaluation of numerous diagnostic and internal test points. The array includes a variety of test cells with direct access emitters, simulated poly load resistors, and direct access points for applying external loads for the purpose of checking unit cell drive range. Probe testing will be conducted using SBIR's new probe station, which incorporates PCI-based digital control data, clock and bias, and data acquisition functions within a single PC-based host.

Emitter pixels will be fabricated using the transferred Honeywell Laboratories emitter process. The process transfer is underway, with Microelectronics Center of North Carolina (MCNC) selected as the transfer foundry. MCNC has been selected due to their demonstrated strength in the areas of MEMS fabrication, process development, and materials science. Pixel design for LFRA is underway, and actual deposition of emitters is expected to start in late 2002.

7 SUMMARY

The LFRA array will demonstrate new levels of IRSP emitter pixel power, and achieve new levels of performance in terms of maximum apparent temperature and radiance rise time. The LFRA capability will support IRSP full field of view (F-FOV) and mobility/portability requirements for installed next generation IR sensors testing the at the US Navy Air Combat Environment Test and Evaluation Facility (ACETEF), the US Air Force Avionics Test and Integration Complex (ATIC), and the US Army Simulation, Training and Instrumentation Command (STRICOM). First silicon will be available for characterization in summer 2002.

8 ACKNOWLEDGEMENTS

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9 REFERENCES

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