Achieving Ultra-high Temperatures with a Resistive Emitter Array

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ABSTRACT

The rapid development of very-large format infrared detector arrays has challenged the IR scene projector community to also develop larger-format infrared emitter arrays to support the testing of systems incorporating these detectors. In addition to larger formats, many scene projector users require much higher simulated temperatures than can be generated with current technology in order to fully evaluate the performance of their systems and associated processing algorithms.

Under the Ultra High Temperature (UHT) development program, Santa Barbara Infrared Inc. (SBIR) is developing a new infrared scene projector architecture capable of producing both very large format (>1024x1024) resistive emitter arrays and improved emitter pixel technology capable of simulating very high apparent temperatures. During earlier phases of the program, SBIR demonstrated materials with MWIR apparent temperatures in excess of 1400 K. New emitter materials have subsequently been selected to produce pixels that achieve even higher apparent temperatures. Test results from pixels fabricated using the new material set will be presented and discussed. A 'scalable' Read In Integrated Circuit (RIIC) is also being developed under the same UHT program to drive the high temperature pixels. This RIIC will utilize through-silicon via (TSV) and Quilt Packaging (QP) technologies to allow seamless tiling of multiple chips to fabricate very large arrays, and thus overcome the yield limitations inherent in large-scale integrated circuits. Results of design verification testing of the completed RIIC will be presented and discussed.

Keywords: UHT, Infrared, IRSP, HWIL, Scene projection, Hardware in the loop, Through-silicon Via, Quilt Packaging

1. INTRODUCTION

Santa Barbara Infrared (SBIR) is a world leader in the development and production of infrared scene projector systems (IRSPs) that meet the needs of hardware-in-the-loop (HWIL) simulation testing. SBIR's Multi-spectral InfraRed Animation Generation Equipment (MIRAGE) offers the most advanced performance available in resistive array-based IRSPs. As sensor and seeker technology evolves, new performance demands will be placed on the IRSP systems used to test them. SBIR is responding to these demands with the development of the next generation of resistive array scene projector technology. The UHT program is funded by the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the U.S. Army Program Executive Office for Simulation, Training and Instrumentations (PEO STRI). The program's goal is the design, assembly, and test of an updated IRSP system that will offer significant performance increases in apparent temperature, speed and spatial resolution.[1]

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In order to achieve improvements in each of these metrics, development efforts within each subcomponent area are being pursued. New emitter pixels that leverage the basic design foundation of existing MIRAGE pixels, but incorporate new materials and geometries, have reached the program goal of 1500 K apparent temperature in the MWIR band (3.0 – 5.0 μm) during testing, corresponding to an in-band radiance of 2.47 W/cm^{2}sr. In addition, the design of a new read-in integrated circuit (RIIC) that will support a faster frame rate requirement of 500 Hz and the increased power required by higher temperature pixels has also been completed. The design of this RIIC supports array quilt packaging, in which multiple smaller RIIC tiles are packaged together to produce one composite larger emitter array. The first 3-side quiltable RIICs, which will verify key design elements of 4-side quiltable RIICs, have been fabricated and tested.

2. BACKGROUND AND GOALS

The UHT program calls for advancement in essentially every performance metric that characterizes a resistive array-based IRSP. This includes increasing the maximum MWIR apparent temperature from 700 K (0.13 W/cm^{2}sr) to over 1500 K (see Figure 1), increasing the maximum frame rate from 200 Hz to 500 Hz, and supporting array formats of up to 2048 x 2048 pixels. During the first phase of the program, emitter pixels incorporating new materials and geometries were fabricated and tested.[2] These pixels produced significantly more radiance than legacy pixels, and the data collected drove additional design modifications for the second program phase. In the second phase of the program, the material set for the pixel was refined based on the experiences from the first phase, and tested both in a bulk film anneal to over 1500 K and in individual test structures. Early second-phase pixels incorporated improvements in photolithography (resulting in improved fill factor) and geometric designs that had been identified by finite element analysis (FEA) as likely to respond best to thermo-mechanical stress. The first batch of pixels tested in this phase approached the program goal of 1500 K, and improved upon the MWIR radiance of legacy designs by a factor of nearly 20x.[3]

After the large-array trade study confirmed QP as the optimal path to larger and faster emitter array formats, a new read-in integrated circuit (RIIC) design was initiated and completed.[3,4] This baseline design consists of a 512 x 768 tile size built up from modular stitch blocks, and incorporates QP nodules on 3 of its 4 sides. The fourth side features conventional bond pads for signal input/output, while power and ground are routed through the backside via TSV's. RIICs using this design will be used as tiles to build a scalable array with N x 512 columns and up to 1536 rows (N x 2 tile format), and thus will provide an effective platform for testing the technologies that will ultimately be used to produce 4-sided quiltable RIICs for even larger array formats. SEM imagery of test designs confirmed that sub-pixel alignment and spacing between tiles can be achieved, which will prevent artifacts in the projected imagery at the tile boundaries. Simulations performed on the 512 x 786 RIIC design confirmed that the RIIC can achieve the desired 500 Hz frame rate and deliver up to 3.2 mW per pixel. With the current configuration that relies on TSVs for power routing, the design is expected to achieve a spatial power variation of less than 1%, even with a significant fraction of the array driven to maximum power.

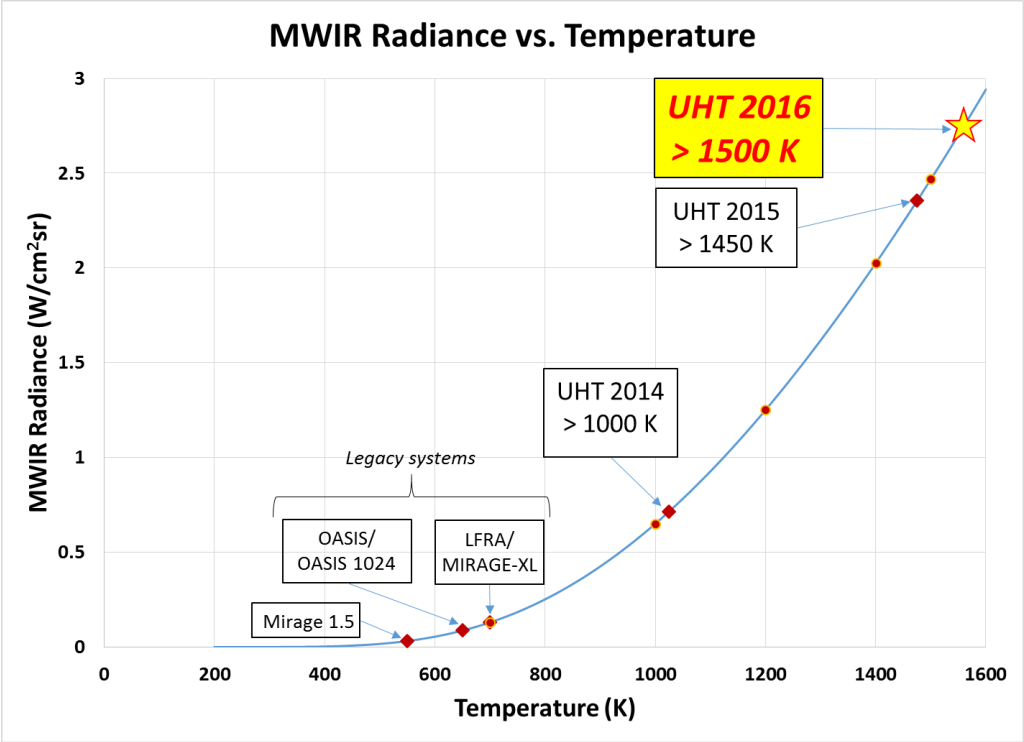

Figure 1. Maximum MWIR radiance and apparent temperature performance of legacy IRSPs and evolution of UHT pixel performance across program phases.

3. UHT EMITTER PIXEL TESTING RESULTS

Further design improvements were determined based on the test results and subsequent analysis of the early-phase pixels. Figure 2 highlights the key pixel structural components for reference. It was determined that even higher temperatures could be achieved by applying modifications to the layering order and refinements to the leg-emitter interface. Additional modifications were made to the materials set and manufacturing process to further improve pixel response to thermo-mechanical stress. The pixel geometries that produced the best results in early-phase testing were carried forward, and new pixels with these geometries incorporating these improvements were produced.

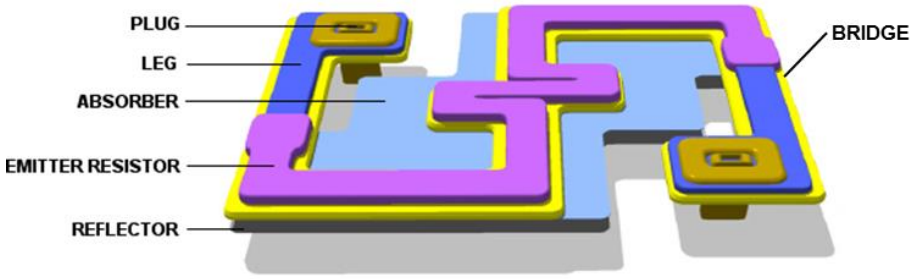

Figure 2. Conceptual drawing of pixel structure showing key components that are responsible for electrical (leg and resistor), mechanical (plug and bridge) and optical (absorber and reflector) performance.

The completed and packaged pixels were electrically and radiometrically characterized at SBIR using a turnkey Calibration and Radiometry System (CRS). The CRS includes a MWIR camera that was calibrated using a flood source. Additional camera characterization for imaging high-temperature point sources came from measurements of a 1000C cavity blackbody with a pinhole aperture. The use of a cavity blackbody and aperture wheel for high temperature measurements prevented inaccuracies from flood source warming of the camera and its optics at high temperatures. Pixels from the latest batch reached significantly higher temperatures than the early-phase pixels, and pixels from two different designs achieved the 1500 K radiance target. In addition to the pixels that exceeded 1500 K, pixels from several different designs exhibited maximum temperatures between 1400 K (2.03 W/cm^{2}sr) and 1500 K with good thermal and electrical stability. Thermo-mechanical stress was identified as a likely limiting factor for the maximum attainable radiance for a given design. The Figure 3 shows the maximum radiance reached by the better-performing designs.

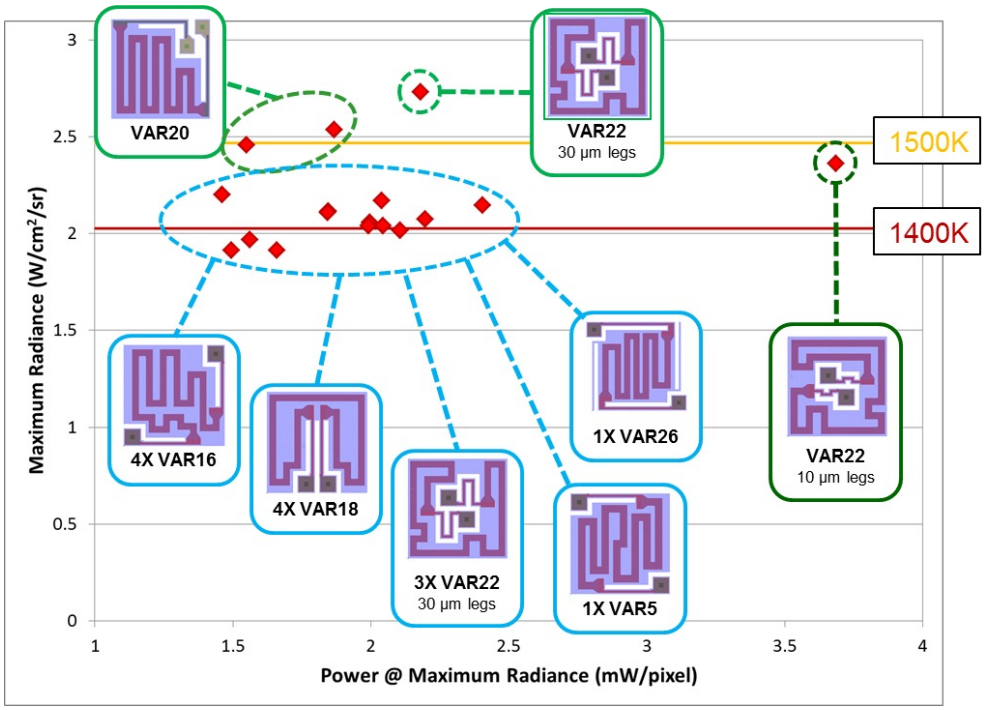

Figure 3. Pixel geometries from Lot 2b that achieved the highest MWIR apparent temperatures.

Pixels with the most promising design geometries were further tested to verify reasonable power consumption and structural stability at high temperatures. Figure 4 shows the radiance as a function of power applied to one of the pixels over the course of multiple excursions from ambient to high temperatures. The maximum power consumption for this pixel was approximately 1.6 mW, which is significantly less than the 3.2 mW per pixel that the UHT RIIC is capable of delivering, and was typical of the peak temperature power consumption for the best pixel candidates. The latest tested pixels demonstrated good survivability at high temperatures. The curve in Figure 4 represents over 1000 significant excursions above ambient background, and indicates that the tested pixel did not experience performance degradation. The two designs that demonstrated the best radiance and stability performance were identified as the best candidates for producing a full array.

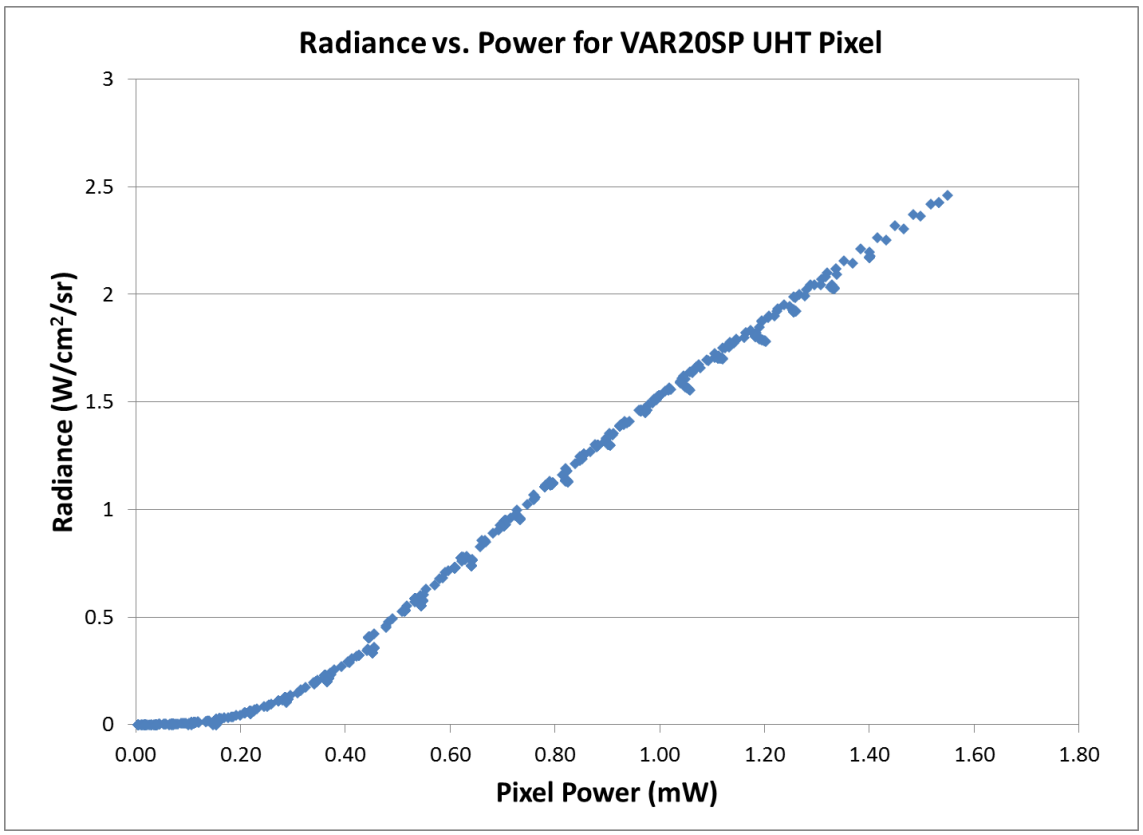

Figure 4. Radiance as a function of applied power to a VAR20SP pixel from the latest round of testing. Each point represents a separate temperature excursion from ambient, constituting over 1000 excursions for this individual pixel.

4. RESULTS FROM UHT RIIC TESTING

Design Verification Testing (DVT) of the first UHT RIICs was performed using the SBIR wafer probe station with a custom probe card, and provided a thorough test of all RIIC functions. DVT included verification of the RIIC power-up sequence, and measurement of chip power consumption after power-on. The power dissipation measurements confirmed the RIIC's low operational power demand. The RIIC design includes four buffered row scan output signals that indicate RIIC response to control signals. The expected scan output pulse width was confirmed during DVT, and the scan output was monitored during further testing to verify probe contact and signal integrity. RIIC operation was confirmed for both operating modes: raster mode (in which the pixel drivers are updated on a row-by-row basis) and snapshot mode (in which the entire RIIC is updated after all values have been loaded). The RIIC's built-in projection interlock mode was shown to successfully protect against unintended array operation, thus verifying an important design safety feature.

In addition to the functional DVT tests, the response of the RIIC to changes in frame rate and input signal voltage were measured. As shown in Figure 5, the current draws for the digital and analog bias lines to the card both display linear relations to the frame rate, as predicted in design simulations. Power consumption is reasonable, with a maximum extrapolated current draw of less than 20 mA at the full 500 Hz frame rate. Similarly, the drive response of the RIIC was verified by varying the signal voltage input to a selected 32-pixel unit cell. For lower input voltages, which correspond to larger input drives in the RIIC's analog architecture, the drive response was verified to be linear.

The maximum expected per pixel current of approximately 800 μA was verified, and the low-drive roll-off from a linear response will help better resolve terrestrial scenes, which typically have an apparent temperature near 300 K.

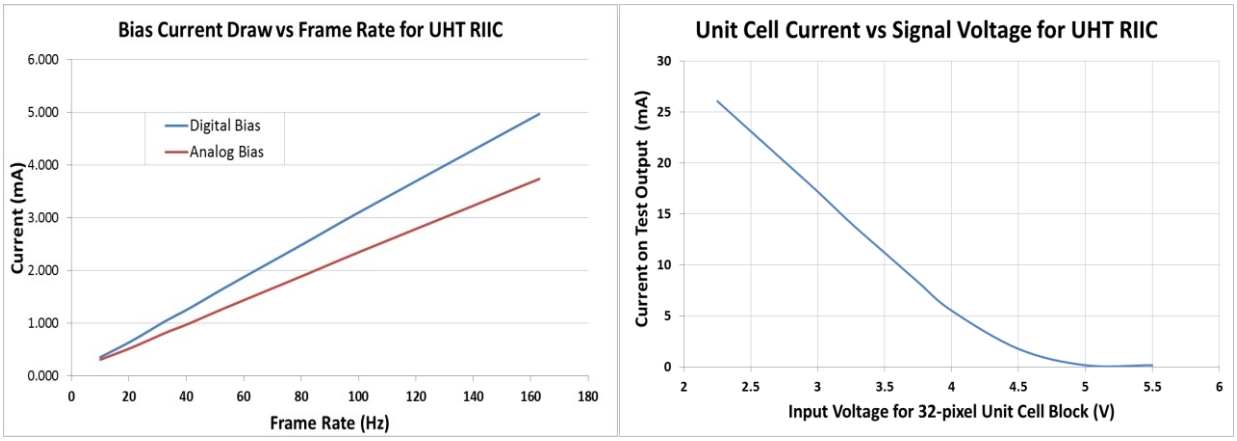

Figure 5 Current draw as a function of frame rate (left), and emitter driver unit cell response as a function of input signal voltage (right) for the UHT RIIC. The output current for the 32-pixel block translates to a maximum per pixel current in excess of 800 μA.

In conjunction with the power dissipation measurement, two additional-full operation tests were performed during RIIC wafer probe screening to identify the candidates most likely to produce a high-quality array. The Analog Input Buffering test was used to verify proper operation of the RIIC circuitry by measuring a voltage input connected to an on-RIIC source follower. Passing devices exhibited an output voltage that scaled with the input, with a level shift at lower voltages and a rollover for input voltages larger than 4.0 V. The Emitter Output test was the most important test for identifying the highest quality RIICs. All emitter pixel drivers were addressed sequentially in 4x6 blocks, and the resulting drive responses of the blocks were used to form an operability map of each RIIC. The unit cell granularity was sufficient to detect abnormalities in a RIIC, including dead rows and columns. Figure 6 shows the operability map of one of the UHT RIICs identified as a high-quality candidate for a full emitter array tile.

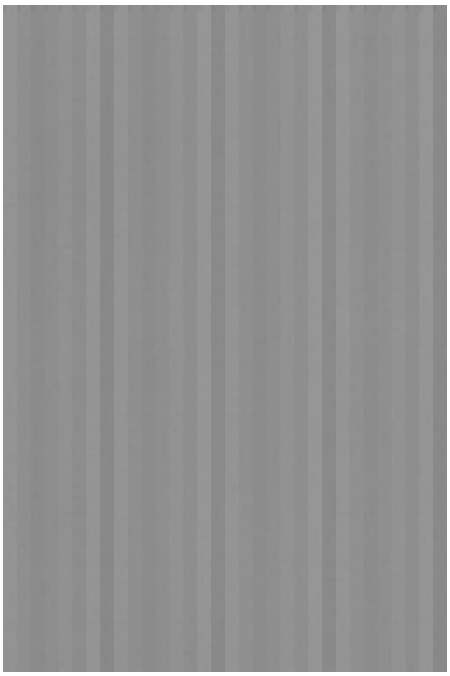

Figure 6. Operability map from the Emitter Output test for a UHT RIIC passing Design Verification Tests and identified as a candidate for a high-quality emitter array.

5. COMBINED PERFORMANCE OF UHT PIXELS AND RIIC

Given the large thermal range that will be covered by the full UHT system, thermal resolution becomes an important system-level consideration. It is highly-desirable that the system produce a well-resolved thermal background near ambient temperatures (approximately 300 K), which requires a thermal resolution (minimum step size) of better than 0.1 K[5]. Figure 7 shows the radiance as a function of input current for one of the pixels that achieved the 1500 K target. At maximum radiance, the current draw from the pixel was 625 μA, which is well within the capabilities of the UHT RIIC. The measured pixel radiance as a function of current can be combined with the drive response of the RIIC measured during DVT (Figure 5) to determine the pixel response behavior when married with the RIIC. Given the 14-bit RIIC architecture, the thermal resolution of the RIIC has been predicted, and also shown by the right-hand plot in Figure 7. Over the entire output range, the resolution of the system is predicted to be much better than 0.5 K, and more importantly, to be less than 0.1K near terrestrial background temperatures (~300K).

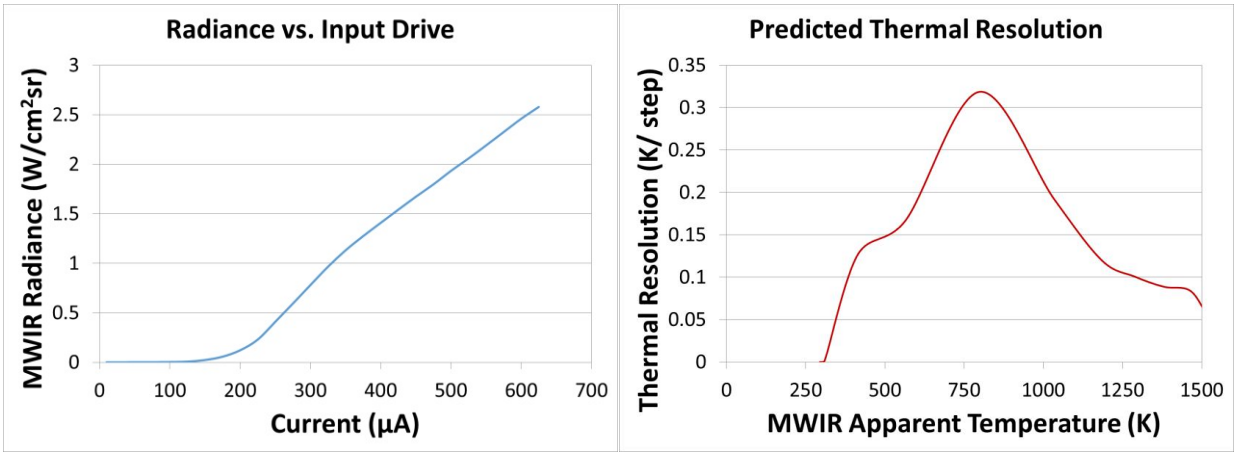

Figure 7: Radiance as a function of input current for one of the pixels that achieved the target radiance (left). The pixel response to current was combined RIIC drive response curve in Figure 5 to predict the pixel behavior in the RIIC. The 14-bit RIIC architecture results in a thermal resolution shown in the figure on the right.

6. SUMMARY

In response to evolving customer needs, advancements in the performance of key IRSP subcomponents have been made, and the performance of these critical building blocks of a complete next-generation IR scene projector system have been verified. The most recently tested emitter pixels have produced the highest measured radiance to date from a resistive emitter pixel, and have achieved the MWIR apparent temperature goal of 1500 K. Pixels with several different geometries achieved high temperatures and demonstrated robustness under repeated testing. The new RIIC that will drive these pixels has been fabricated and tested at SBIR. The completed RIIC design passed all DVT and operational tests, and has been proven capable of providing the power and current needed to drive the new pixels to maximum radiance. This 512 x 768 pixel format chip will make use of TSVs and quilt packaging technology to create the first multi-tile composite emitter arrays. Parallel design efforts for drive electronic design and packaging have made promising progress, and are expected to be complete within the next year. Upon their completion, these efforts will provide all of the necessary components to produce the first very-large-format, ultra-high temperature IRSP systems. These systems will achieve the necessary high output radiance targets, while simultaneously providing the fine thermal resolution needed to maintain important details in an ambient background scene.

7. REFERENCES

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