OASIS: Cryogenically-Optimized Resistive Arrays & IRSP Subsystems for Space-Background IR Simulation

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ABSTRACT

SBIR has completed design and development of prototype emitter arrays and is completing custom cryogenic vacuum device packaging and support electronics for the Optimized Arrays for Space-background Infrared Simulation (OASIS) program. The OASIS array is a 512 x 512 device featuring high output dynamic range, a selectable analog/digital scene data interface, and the capability to operate from cryogenic to ambient substrate temperatures – thereby providing an enabling technology for projection of simulated radiance of space-background scenes. Prototype emitter production has been completed at RTI International in support of initial deliveries. The OASIS array package incorporates novel electrical bussing schemes optimized for the OASIS RIIC and a modular architecture to allow user re-configuration of both window and emitter shield. The OASIS package leverages LFRA operation features, and supports both ambient and cryogenic chamber-based operation with a minimum of mechanical and electrical re-configuration. The OASIS close support electronics (CSE) supports both analog and digital input data modes, while providing easy electronic connection between arrays installed in the cryogenic chamber and the external control and scene-generation systems. We present a technical overview of the OASIS array/package and CSE designs, and will report on measured radiometric performance from prototype OASIS arrays.

Keywords: Command & Control Electronics, Emitters, Hardware-in-the-Loop Simulation, IR Scene Projection, Electronic Packaging, MEMS Fabrication, OASIS, KHILS.

INTRODUCTION

SBIR entered into IR Scene Projection (IRSP) in 1999 and has made significant investments in IR Scene Projection (IRSP) technology. SBIR has an exclusive position in resistive IRSP with more than 15 fielded systems worldwide, and continues to advance the state-of-the-art with LFRA, OASIS, MIRAGE II and WFRA products.

Next-Gen IRSPs are pushing the state-of-the-art with Higher T_{max} (> 700 K), faster rise time (< 5 ms), larger formats (768 x 1536), and low background (50 K), as illustrated in Figure 1. Future systems demand new device designs and material choices:

- High RIIC drive power levels
- Advanced RIIC processing
- Advanced emitter materials
- Low-impedance emitter supply/return bussing
- Novel emitter design/layout
- Low background simulation/cryogenic operation

SBIR embarked on the OASIS program in 2004 to develop and produce improved next-generation cryogenic arrays for low background scene simulation. Prototype OASIS emitter fabrication has been completed, and back-end assembly and command and control electronics are in process.

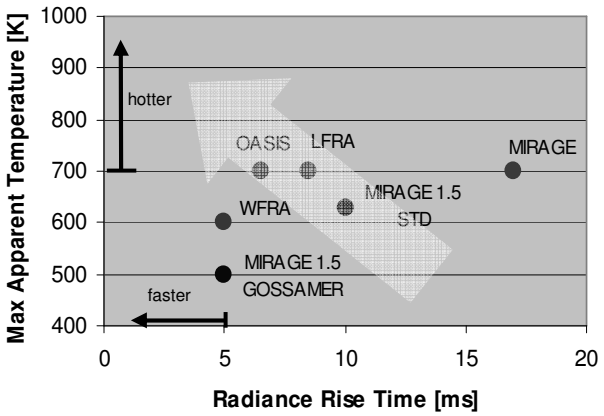


Figure 1 – Performance Evolution of SBIR IR Scene Projector Products

1. EMITTER DESIGN & FABRICATION

The OASIS program has developed a new generation of resistive emitter arrays optimized for cryogenic IR scene projection. OASIS has evolved the state-of-the-art in cryogenic projection, leveraging previous development programs such as the Nuclear Optical Dynamic Display System (NODDS). OASIS represents a significant improvement in operational performance and affords the Hardware in the Loop (HWIL) test community a significant new infrared simulation device optimized for cryogenic use in support of missile defense simulations.

A number of features in the LFRA emitter pixel design and fabrication were leveraged for OASIS. Both LFRA and OASIS use a pixel pitch of 48 µm, with OASIS utilizing a 512 x 512 array configuration. The OASIS emitter unit cell is stepped in both x and y, to match the layout of RIIC core. The pixel layout was optimized for the best combination of temperature, speed, and performance margin. The mask set incorporates a variety of low-risk improvements leveraged from LFRA. In order to achieve rise time (0-90%) to < 6.5 ms for OASIS, the pixel leg length was set to 18 µm. Optical fill factor for OASIS was designed for 52%. For comparison, Figure 2 shows the pixel design layout and an optical micrograph of a finished OASIS pixel.

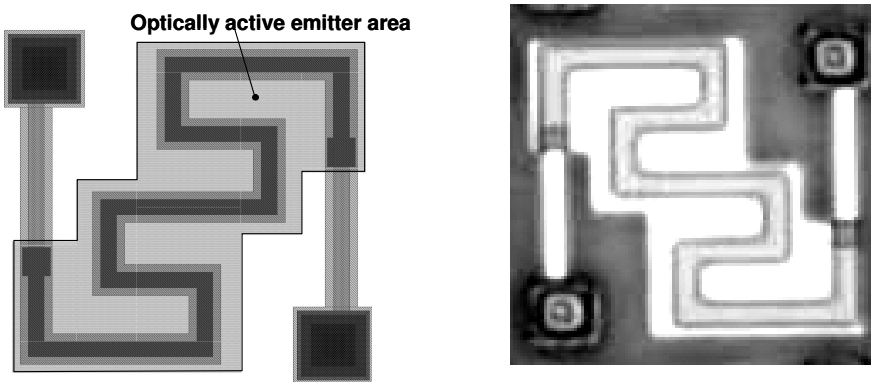


Figure 2 – OASIS 48 µm Pixel Layout

For OASIS emitter fabrication, ten 100 mm wafers started into the SBIR/RTI emitter process line. The first run yielded 33 Grade "A" emitter arrays. Of these, 12 arrays have pixel operability's estimated at > 99.9%. All other inspection criteria were met.

Emitter Process Improvements

Significant OASIS emitter process development resulted in key improvements to cryogenic resistance coefficient measurement, wafer coring, and implementation of an advanced tungsten post array CMOS interface.

Wafer coring proved challenging as the goal for high yield demands maximum survival of the wafers throughout processing. Key to this survival is the elimination of cracks originating from edge chips during coring. These edge chips can either result in localized die attrition or catastrophic loss of the cored wafer. Coring is performed to reduce a 200 mm diameter wafer into smaller 100 mm diameter wafers better adapted to further device processes each with 4 grade A dice as illustrated in Figure 3.

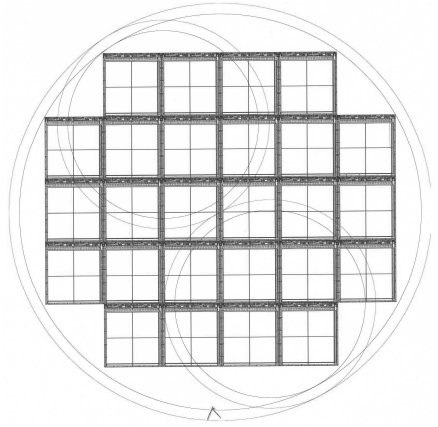


Figure 3 – OASIS Wafer Coring Layout

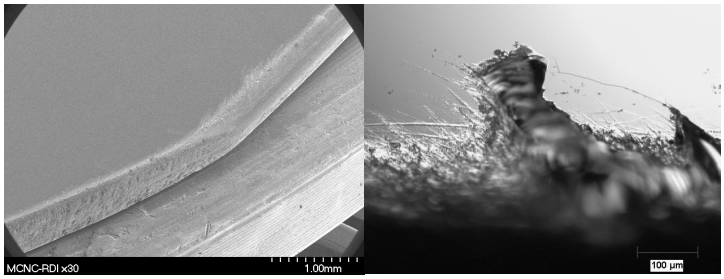


Figure 4 – Edge Condition and Flaws from Coring

Laser coring, water-jet assisted coring and micro-abrasive blast techniques were all investigated in order to improve coring yield. Laser coring produced the sharpest edges, which ultimately created problems during subsequent cleaning and handling steps. Micro-abrasive blast – although unsophisticated – produced uniformly round edges exhibiting a shallow depth of subsurface damage that held up the best during subsequent wafer process steps.

CMOS Interface Improvements

One of the key process improvements realized on OASIS is that of the tungsten post array interface to the CMOS RIIC. The tungsten post array CMOS interface (see Figure 5) is considerably simpler to implement than the previous "top-metal passivation cut" approach. In this approach, CMOS wafers are delivered from the foundry with a planarized top surface and tungsten post contacts covered by only a thin dielectric layer. The subsequent deposition of reflector-contact metal results in excellent CMOS-to-emitter interconnection. SBIR and RTI have had considerable success in adapting this interconnect scheme for use with their tool-set and internal processes.

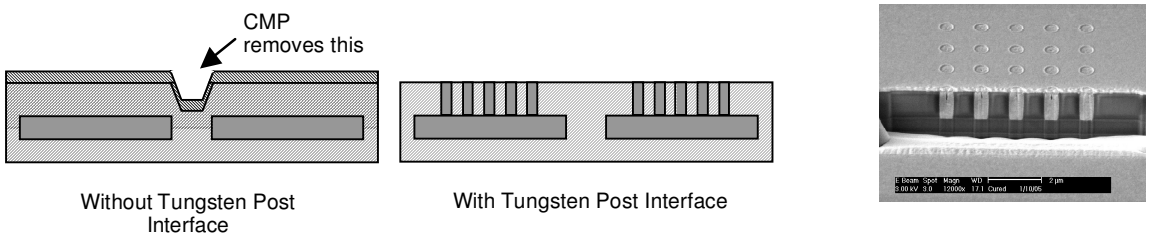


Figure 5 – Tungsten Post Array CMOS Interface

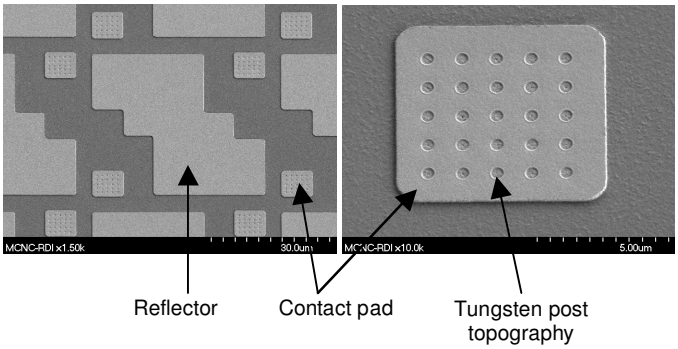
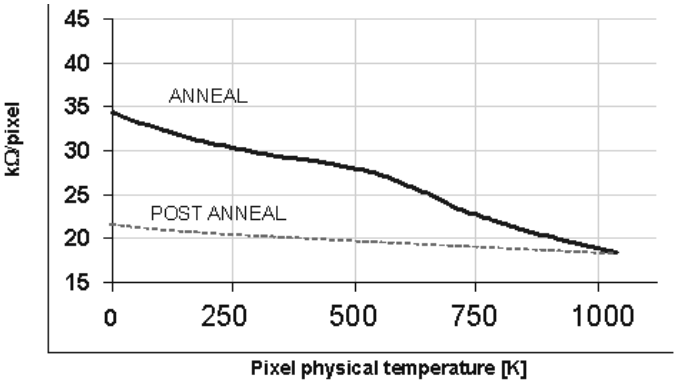


Figure 6 – Metal Reflector/Contact Pad Configuration

2. PIXEL ANNEALING

The design goal for post-anneal emitter resistance is 20 kΩ/pixel. This value determines the maximum temperature for a given unit cell drive circuit and overall affects the maximum array power dissipation. Anneal characteristics were obtained on pixel equivalent test structures. A summary of results to date are shown in the following graph of resistance as a function of physical temperature as the current is ramped 0-150 µA/pixel. An "as deposited" to "post anneal" resistance ratio of 0.6:1 was obtained – consistent with the previously-validated anneal curve characteristic.



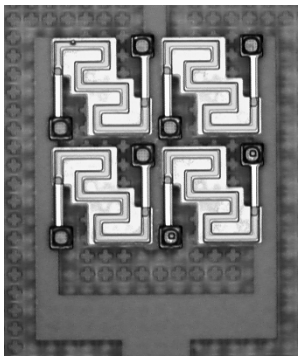


Figure 7 – OASIS Pixel Anneal Characteristics and 2 x 2 test structure

As deposited sheet resistance was lower than anticipated. Results of wafer runs are given in Table 1. Based on this outcome, compensation was achieved by reducing line width in photolithography. Though this necessitated an extra mask set, it represented a cost-effective technical solution and provided a variety of process development benefits.

Batch Summaries (kΩ/pixel)			
	Batch 1	Batch 2 (std litho)	Batch 2 (thin LW)
Average	30	31	29
Max	37	35	31
Min	27	25	28
Target	33	26	33

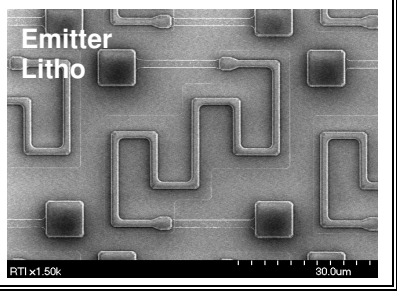


Table 1 – As Deposited Sheet Resistance Summary

3. PERFORMANCE

While fill-factor and post anneal resistance directly affect maximum apparent temperature of the emitter pixel for a fixed pixel mass, its thermal conductance directly affects rise time. Rise time is inversely proportional to conductance, while rise time is directly proportional to leg length. OASIS leg length is 18 µm which resulted in 0 to 90% rise times of approximately 6.5 ms, as illustrated in Figure 8.

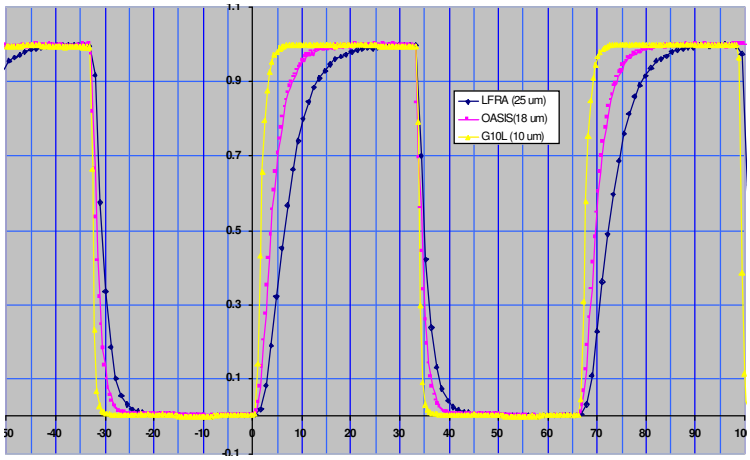


Figure 8 - Rise Time Characteristics as a Function of Leg Length

4. SYSTEM DEVELOPMENT

The OASIS system is composed of three main sub systems: the Cryogenic Projector/Electronics Module (Cryo-PEM), the Command and Control Electronics (C&CE) and the Thermal Support System (TSS). The Cryo-PEM package contains the emitter array, opto-mechanical interface, Close Support Electronics Module (CSE), and electrical interface and proximal electronic cards. The CSE controls power input, ground, signal and power conditioning, and several test and telemetry functions.

Cryogenic Projector/Electronics Module (Cryo-PEM)

The Cryo-PEM package design meets both external and internal specifications in order to properly support and condition the emitter array. Primary considerations for the package design were provision of a high conductance thermal path from die to sink, a low electrical impedance (resistance and inductance) electrical path to the CSE, a physical form factor compatible with the basic Honeywell-legacy package, and support for close butting in two-color projection applications, as illustrated in Table 2.

Key Cryo-PEM features include ambient and 50 K operation capability, a custom multi-layer ceramic (MLC) emitter array chip carrier package, an interchangeable window interface, a meso-channel fluid plenum cooler used for ambient operation, a small overall physical form factor (~ 80 mm/side), support for vacuum operation and low residual out-gassing, and high emitter reliability.

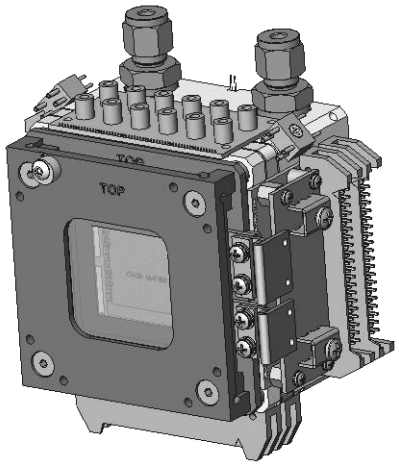


Figure 9 – OASIS Cryo-PEM

Array Configuration	512 x 512 48 μm pixel pitch
Operational Temperature	50 K – 320 K
Thermal Load	125 W (Steady-State) 300 W (Peak)
Electrical Load	25 A (Steady-State) 50 A (Peak)
Emitter Window	Broadband (3-12 μm) Replaceable
Cold Shield	Aperture Only Optimized for f/1.5-f/6.6
Physical Interface	Flat Mount – Back Surface
Electrical Interface	Close Proximity Analog/Digital boards

Table 2 – OASIS Packaging Specifications

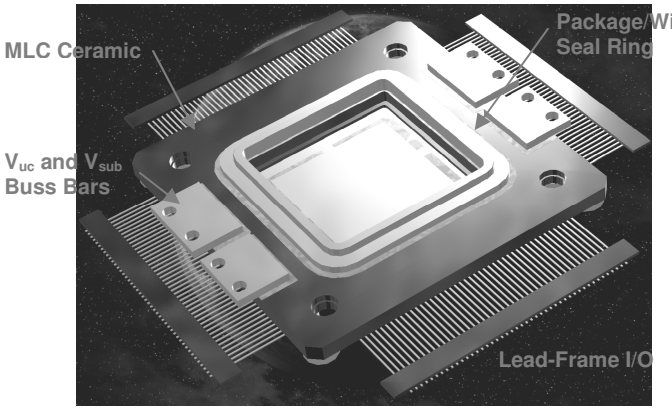
The OASIS Cryo-PEM has significantly lower thermal resistance than the legacy HTC package over the operational temperature range – and represents an approximate 10x improvement at 50 K. In-plane thermal non-uniformity has been virtually eliminated due to high diffusivity and proximity of the heatsink and heat spreader to the die. Thru-thickness thermal resistance is approximately 0.029 K/W at 50 K. The use of CTE matched materials supports soldered construction of die attach and chip carrier to heatsink assembly, thereby enhancing both heat transfer as well as vacuum integrity.

Multi-Layer Ceramic (MLC) Chip Carrier

The MLC chip carrier is a 228 lead CQFF package. The OASIS package provides the primary electro-mechanical interface for the die to the Cryo-PEM. The package features a heatspreader, integral metal vacuum seal ring and mounting feet, MMC high current and ground bus bars, internally-routed traces for electrical interconnection, gold wire bonds, and optimized cryogenic construction techniques for high reliability per MIL-STD-883.

Heat Spreader

For dielectric heat transfer materials, BeO, diamond MMC, AlN, sapphire, and other materials were considered for use as a heatspreader. At 50 K, sapphire has one of the highest thermal conductivities of known materials, and represents an excellent choice for cryogenic only operation – however, its conductivity drops dramatically to 40 W/m/K at 300 K. As OASIS operates from 50-320 K, the other materials afford significantly lower thermal resistance than sapphire, whilst maintaining an acceptably high thermal conductivity at 50 K.



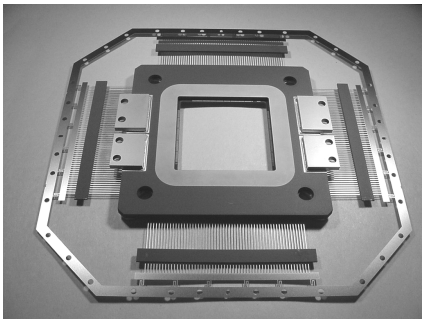


Figure 10 – OASIS MLC Emitter Array Chip Carrier Figure 11 – Finished MLC Chip Carrier

Electrical connections between the chip carrier and the CSE are made via four paddle-boards attached to the sides of the Cryo-PEM heatsink. A lead-frame electrical interface to the MLC chip carrier was chosen for OASIS to promote ease of assembly with the close proximity paddle boards located at right angles to leads, and provides a direct electrical interconnect. This promotes high reliability throughout temperature cycling.

Ambient Test Fixture

Ambient operation and storage is facilitated by the SBIR ambient test fixture. This compact test stand features a miniature ion pump, manual bellows vacuum valve, interface mount, and a physical form factor equivalent to that of the HTC Legacy Cryo-PEM test fixture.

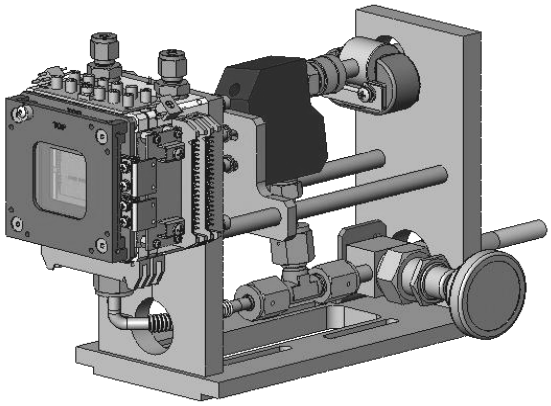


Figure 12 – OASIS Ambient Test and Storage Fixture

During operation at ambient temperatures, heat transfer fluid may be circulated through the Cryo-PEM via fittings accessible on top of the heatsink. The brazed heatsink assembly has a unique integrated all-copper meso-channel cooler, which facilitates heat transfer with the MLC chip carrier heat spreader and maintains a stable emitter array temperature. The heatsink is compatible with many popular heat transfer fluids. The cooler thermal resistance, R_{th} = 0.019 K/W, achieved for water at T_{inlet} = 293 K and 4 lpm flowrate, supports the operational capabilities of the emitter and can remove over 300 W of dissipated power. The cooler is also LHe compatible.

The emitter array is maintained in a local vacuum environment during operation and storage. The die cavity in the MLC chip carrier is sealed by the optical window using a single, low-permeable o-ring, and may be pumped either directly using a separate vacuum pump system or the mini-ion pump provided on the ambient test fixture to a level < 1E-04 torr.

Close Support Electronics (CSE)

The Close Support Electronics (CSE) for OASIS provides for a flexible scene data path and is based on the LFRA architecture. Figure 13 illustrates a simplified layout of the CSE in the OASIS system.

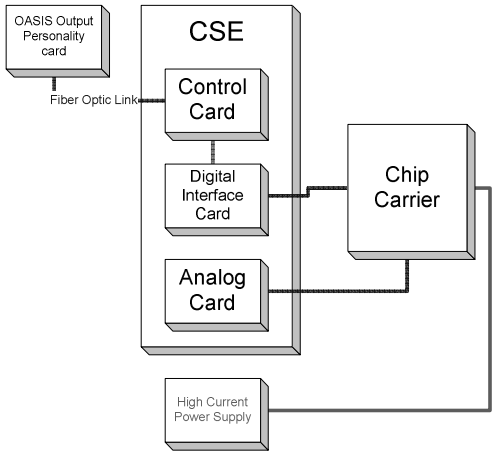


Figure 13 – OASIS CSE Architecture Schematic

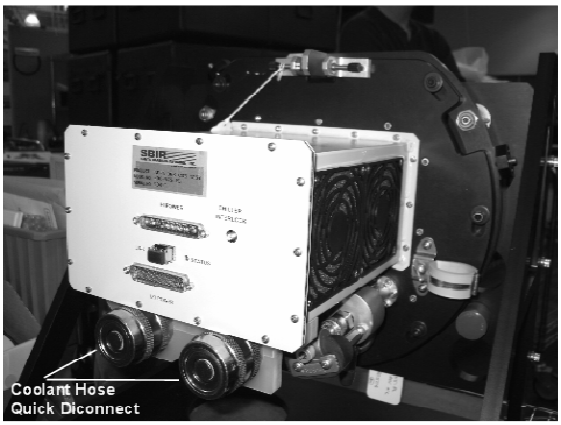


Figure 14 – Production LFRA CSE

The CSE is located between the Cryo-PEM and the C&CE to provide the main electronic and signal interface to the emitter array. Both digital and AIE drive modes are supported. Due to the nature of cryogenic operation, a long physical cable run must be accommodated, thereby posing a variety of inductance-related interface challenges. This has been mitigated through careful buss bar design and power conditioning local to the close-proximity paddle boards.

Thermal Support System (TSS)

The Thermal Support System (TSS) for OASIS leverages the LFRA production hardware. It is used as the primary power source for the emitter as well as providing control of RIIC die temperature during ambient operation via a separate chiller. During cryogenic operation, a separate LHe system is used to cool the Cryo-PEM down to 50 K via a conduction plate and thermal straps. A thin-film heater mounted on the back of the Cryo-PEM controlled from the TSS provides for fine temperature control (± 1 K) of the RIIC die temperature.

Figure 15 – LFRA/OASIS Thermal Support System (TSS)

Command & Control Electronics (C&CE)

The OASIS C&CE receives user scene data from the scene-generation platform, performs a variety of real-time DSP functions, provides a GUI for system control, displays pre- and post-processed real-time imagery, and transmits projector data to the Cryo-PEM CSE via a fiber optic interface. The past year has seen completion of the LFRA IRSP system, upon which the architecture of the OASIS C&CE will be built. OASIS-specific modifications will involve completion and checkout of the OASIS Output Personality Processor (OPP) board as well as firmware changes. All modifications for the OASIS C&CE are expected to be complete and tested by mid-year 2006.

SUMMARY

The first OASIS production emitter lot was highly successful. Operability greater than 99.9% was obtained with 725 K apparent temperature achieved. Rise time and resistance characteristics met specification. Additional emitter lots are in the process of being integrated into packages for test and evaluation. SBIR's emitter foundry is online with demonstrated processing success, and is running smoothly. The OASIS MLC chip carrier has been completed with Cryo-PEM assemblies and test fixtures currently in fab. CSE electronics development and C&CE design completion are nearing completion.

ACKNOWLEDGEMENTS

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