MIRAGE: large-format emitter arrays 1024x1024 and 1024x2048

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ABSTRACT

The IR detector array, which is the heart of any imaging system or missile seeker, continues to evolve toward larger size, smaller pixels, and higher sensitivity. Any scene projector that is intended to test one of these advanced devices must keep pace. As IR scene projection evolves to 1024x1024 and 1024x2048 arrays, both the emitter array and drive electronics must overcome numerous technological challenges. This paper discusses the approach taken to provide the same 200Hz frame rate, 16-bit accuracy, and high operability already demonstrated with 512x512 MIRAGE arrays in a larger format. In addition to current capabilities that are to be preserved in the design of larger devices, scalability of the architecture to allow growth to even larger formats is desired. Other features such as windowing and even higher frame rates are critical for future applications.

Keywords: Infrared, Scene Simulation, Scene Projection, and Emitter Array

1. INTRODUCTION

This paper describes the technical approach and plan to develop a new generation of Large Area Infrared Scene Emitters (LAISE) based on Government and Industry requirements.

The architecture study performed is based on the desire to extend the existing MIRAGE 512 x 512 emitter array developed by Indigo Systems Corporation and Santa Barbara Infrared, to a 1024 x 1024 and possibly a 1024 x 2048 array configuration. Development of the large format emitter array will involve the scaling up of functions and features originally implemented on the MIRAGE emitter array and the integration of additional features required and desired by the Government.

Under this architecture development study, Indigo and SBIR analyzed the Government and Industry requirements and developed a specification for the large format RIIC. MIRAGE capabilities, which are recommended to be incorporated into this larger format array, are snapshot mode, on-chip D/A converters, high frame rate operation and advanced power modes. New features such as hyperdrive power management mode, high frame rate static window and an all-digital interface are recommended to provide enhanced capabilities for the LAISE.

Presented in this paper are the LAISE requirements, architecture study, and proposed LAISE architecture and specifications. A review of the current MIRAGE architecture and features is recommended prior to reading this paper. An overview of the MIRAGE system is provided in these same proceedings[4].

2. LAISE REQUIREMENTS

2.1 Government and Industry Required Features

The Government and Industry required features are based on expanding the existing MIRAGE 512 x 512 RIIC array and its capabilities to a larger LAISE format 1024 x 1024 emitter array. Table 1 lists the requirements for the next generation of Large Array Infrared Scene Emitters. The 1024 x 1024 array requires square pixels with a size less than or equal to 45 x 45 μm^2. A digital data interface, simlar to the MIRAGE digital interface is also required. This will realized with the on-chip integration of eight digital to analog converters. A frame rate of 200Hz is required for this larger array and will be implemented by having one DAC assigned to each 256 x 512 area of the whole emitter array (integration of eight 16 bit DACs). An apparent 600K temperature dynamic range is required in the MWIR band. The LAISE RIIC is also required to provide the snapshot mode of operation in which frames are simultaneously updated. The rolling mode of emitter display will also be included for scanned systems in which camera line rate can be synchronized to the projector.

Parameter	Requirement
Emitter Array Size	▪ 1024 x 1024
Pixel size	▪ Unit Cell size ≤ 45 x 45 μm^2
Digital Data Interface	▪ 8 on-RIIC DACs (16 bit each)
Frame Rate	▪ 200Hz Frame Rate
Max. apparent To MWIR Max. apparent To LWIR	▪ 600K ▪ 400K
Mode of Operation	▪ Snapshot image ▪ Rolling image loading

Table 1: LAISE required features

2.2 LAISE Desired Features

In addition to the requirements for the LAISE RIIC listed in Table 1, a number of useful modes and functions have been identified that would enhance the emitter array capability, see Table 2. The first of these desired capabilities is an increase in resolution for the emitter array. Some applications will benefit from a rectangular array size of 1024 x 2048 running at 100 frames per second (half the frame rate of a 1024 x 1024 array).

The second capability desired is advanced power management. The LAISE architecture will support both of the MIRAGE power modes; *power-on-demand* and *constant-current.* In addition it is desired to provide a means of combining these modes into a single mode that will seamlessly supply the benefits of the *constant-current* and *power-on-demand* modes. This mode is called the *hyperdrive* mode. In *hyperdrive* mode, a user programmable level of constant current (nominally up to temperatures corresponding to 450K) can be applied to each emitter pixel. In the regime where an emitter pixel's output level and corresponding current requirement is less than or equal to the constant current level, that pixel operates in true *constant-current* operation. In the regime where the emitter pixel's output level and corresponding current requirement is more than the constant current level, that pixel operates in the *power-on-demand* mode of operation. Benefits of the *hyperdrive* operating mode are that the total amount of power that is required by the emitter array can be reduced thus minimizing the overall level of system cooling requirements. The *hyperdrive* modes will preserve much of the constant current immunity to electrical and thermal crosstalk.

Some applications require a higher apparent temperature dynamic range than the baseline LAISE systems requirement. For these systems, a 800K temperature dynamic range is desired in the MWIR band and 450K for the LWIR band. Some applications will also require cryogenic temperature of operation down to 70K. Electrical simulations of the LAISE RIIC will be performed for room and cryogenic temperatures, 300K and 70K respectively. SPICE parameters have been adapted from measurements by Indigo for high accuracy SPICE simulations at 70K.

Fast frame rate capability is also desired for the LAISE emitter array. One possible implementation is a centered static window 1024 x 512 running at 400 frames per second. Dynamic windowing capability is desired. For this mode users desire to have the capability of updating images within a defined window only.

The LAISE RIIC is desired to support an all-digital interface that includes input frame data (8 DACs of 16 bit each) and a serial command register for full digital control of the chip. This will allow further systems simplification.

Parameter	Additional Desire Features
Emitter Array Size	▪ 1024 x 2048 (100Hz Frame Rate)
Power Mode of Operation	▪ Power-on-demand ▪ Constant-current ▪ Hyperdrive
Max. apparent T^o MWIR Max. apparent T^o LWIR	▪ 800K desired ▪ 450K desired
Operating temperature	▪ 330K to 70K
Static Window at 400Hz	▪ Centered static window (1024 x 512) running at 400 frames per second
Dynamic window (programmable size)	▪ Defined at frame rate
All Digital Interface	▪ Digital input for frame input data

Table2: LAISE desired features

3. LAISE ARCHITECTURE STUDY

The architecture proposed for the LAISE emitter array is based on analysis of performance trade-offs resulting in an implementation that addresses the required and desired features identified earlier. Circuit performance (power management, dynamic range and crosstalk), complexity and unit cell size have been studied thoroughly for the design of an architecture including flexible modes of operation with enhanced performance.

Figure 2 shows the floor plan of the proposed LAISE emitter array, which consists of eight blocks (256 x 512 each) with DAC, bias and control logic. The interface is all-digital, with the exception of primary supply voltages, reducing system input requirements. A digital serial command register interface will allow the programming modes for snapshot update, rolling update, *constant-current*, *power-on-demand*, *hyperdrive* modes, high speed static window and tests. Additionally the control of other RIIC parameters including constant current level, maximum emitter current and main bias adjustments will be addressable through this digital protocol.

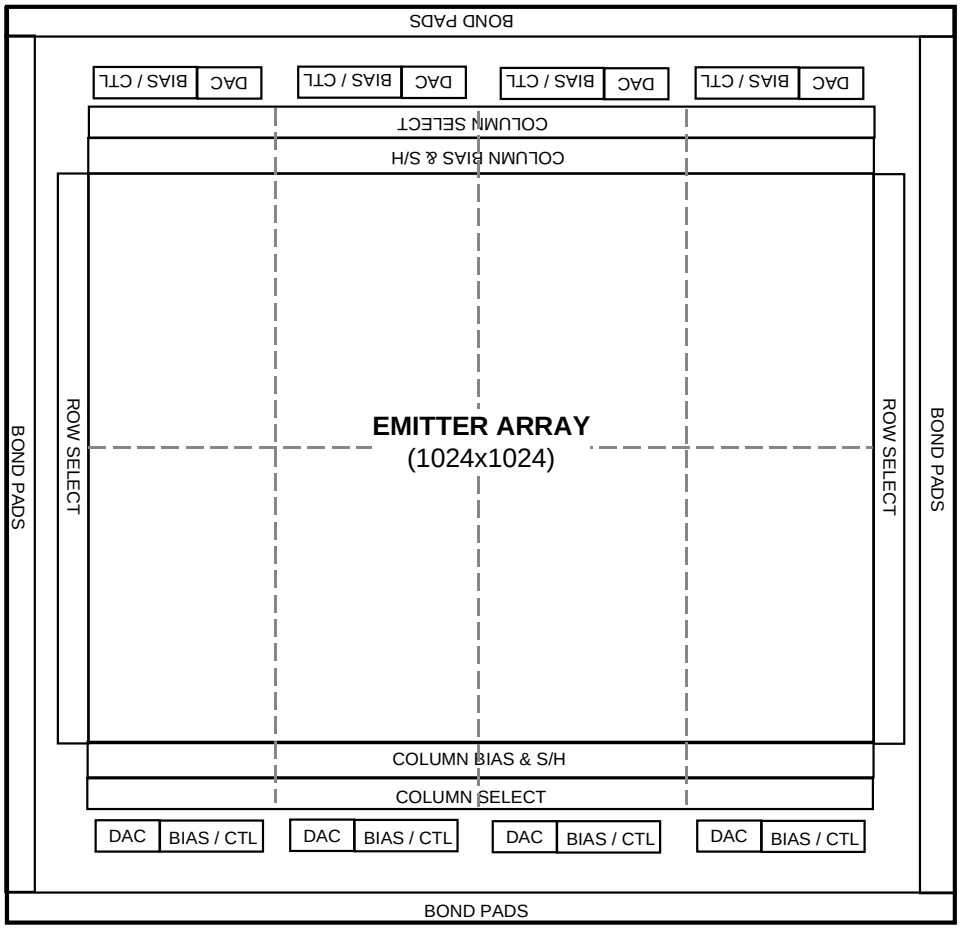


Figure 2: LAISE block diagram, 8 placements of 256 x 512 block with DAC, bias and control logic

3.1 LAISE Snapshot and Rolling Image Display

Like the MIRAGE array, the LAISE emitter array incorporates selectable snapshot and rolling modes allowing flexibility in terms of image synchronization and image stability. The snapshot mode of operation allows the instantaneous display of a frame where all pixels are updated simultaneously to obtain stable images. For the rolling mode of display, the image display is updated on a per row basis. This mode can be useful when the emitter array is synchronized with the line time of the camera.

3.2 Windowing

Windowing capability gives the end user of the LAISE emitter array the full freedom to make trades between frame rate, resolution and total data rate of the scene generation system. Two different windowing methods and implementation are discussed, a fast static window and dynamic windowing.

3.2.1 High Frame Rate Centered Static Window

This mode of operation allows the user to select the central 1024 x 512 area on the array for scene generation at higher frame rates. Figure 3 gives the centered static window configuration. By selecting this mode, the center window of 1024 x 512 pixels can be run at 400 frames per second (each DAC driving half of its corresponding sub-block array

only). The background edges of the array can be either set to zero (substrate temperature) or an arbitrary background scene which may be updated at a much lower frame rate, 1 to 10 Hz for example. This will allow control of the edge effects at the periphery of the centered static window. Scene droop of less than 1% has been measured for 0.1Hz frame rate. This centered window can be used to cut back the input data rate by a factor of two for the 200Hz frame rate operation.

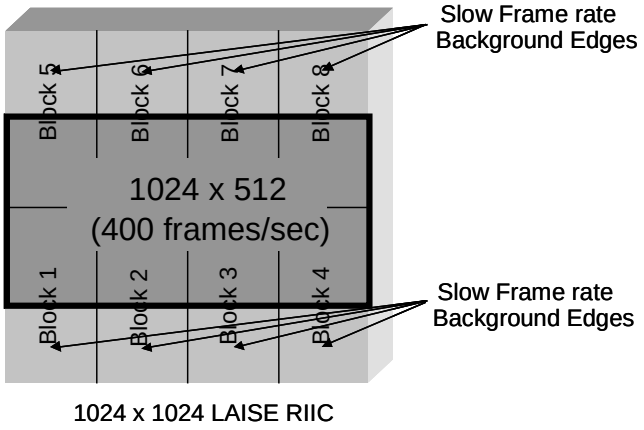


Figure 3: LAISE Static Windowing

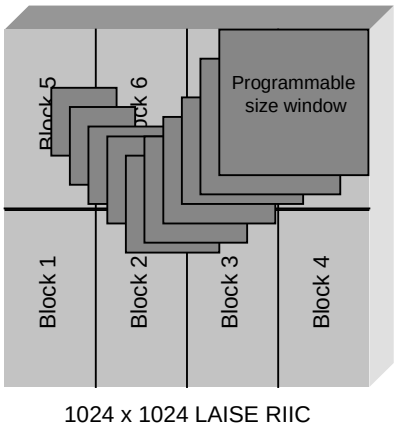


Figure 4: LAISE dynamic windowing generated at the system level

3.2.2 Dynamic Windowing

Dynamic windowing, represented in is known to be a desired feature of next generation scene simulators. Dynamic windowing is desired as a method to reduce the data throughput rate required to drive a full 1024 x 1024 (or larger) array, while maintaining the full field of projection of the emitter array. Dynamic windowing allows the dynamic parts of the full scene to be updated at a 200Hz frame rate while updating the unchanging portions of the scene at a much slower rate; perhaps as slow as 1Hz. While this feature can be implemented into the RIIC design by implementing random access read-in capability, careful considerations of impacts to system and RIIC level design indicate that this feature can be implemented more efficiently at the system level digital processing electronics. Implementation of dynamic windowing in the signal processing electronics in no way limits the performance of dynamic windowing, while freeing up room in the RIIC unit cell for implementation of other features.

3.3 Power Handling Modes

The LAISE emitter array has three selectable power handling modes: *power-on-demand*, *constant-current* and *hyperdrive* modes.

3.3.1 Scene Based Power Mode (*Power-on-Demand*)

In the default mode of operation, *power-on-demand* mode, the unit cell power, defined by the input data value, is proportional to the emitter temperature set via the DAC (i.e. scene based power). Programming the maximum emitter current through an on-chip 4 bit DAC (via the digital control interface) controls the maximum power dissipation allowed, 480W for the 1024 x 1024 array. Limiting the maximum power ensures that the emitter will not be operated in a way that could cause damage through overheating.

This mode of operation can generate a scene related crosstalk when an emitter or a large group of emitters draws a large amount of current. The voltage drop along the supply lines across the array, due to the emitter current, can produce scene related crosstalk seen along the supply bus line ("bus-bar robbing" effect). Furthermore, the instantaneous power dissipated in the RIIC substrate by a group of emitters can also generate a thermal crosstalk (or spreading) due to emitter substrate temperature variations. Final routing analysis of the LAISE layout will define the amount of scene related crosstalk (or "bus-bar robbing"), which is expected to be more than the 0.5% requirement (depending on the scene data).

3.3.2 Constant-Current Mode

The LAISE architecture incorporates a proprietary *constant-current* circuit in each unit cell to ensure that unit cell power is constant over the emitter temperature range. There are two primary benefits from this mode of operation. The first of these is constant unit cell power dissipation, which provide a uniform and stable substrate temperature. This improves the radiometric characteristic of the device. Secondly, the *constant-current* mode virtually eliminates the scene related crosstalk or "bus-bar robbing" effect due to the constant current flowing into each unit cell. The constant-current level is programmed through an on-chip 4 bit DAC limited to a maximum power dissipation of 480W. A maximum of 2% power dissipation difference is expected between all emitter pixels OFF and all pixels displaying the maximum output level.

3.3.3 Hyperdrive Mode

A major feature added to the existing capabilities is the *hyperdrive* mode. The *hyperdrive* mode blends the features and benefits of the *constant-current* mode and *power-on-demand* mode, Figure 5. In *hyperdrive* mode, a user programmable level of constant current (nominally up to temperatures corresponding to 450K) is applied to each emitter pixel. In the regime where an emitter pixel's output level and corresponding current requirement is less than or equal to the constant current level, that pixel operates in true *constant-current* operation. In the regime where the required emitter drive current exceeds the constant current level, the additional amount of emitter current will automatically be supplied to that pixel in a *power-on demand* basis.

There are several benefits to the *hyperdrive* operating mode. First, the total amount of power that must be delivered to the emitter array can be limited to reduce the overall system level cooling

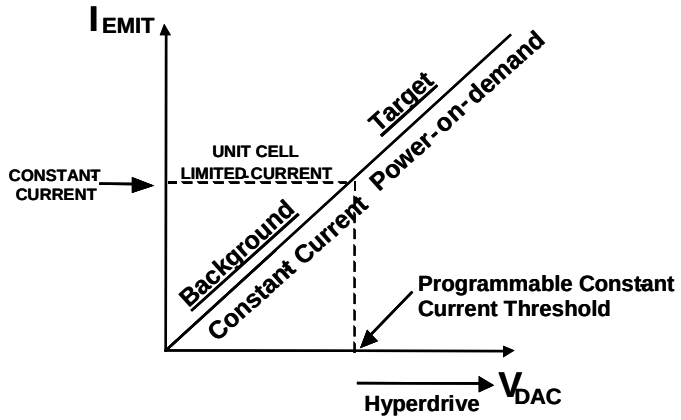
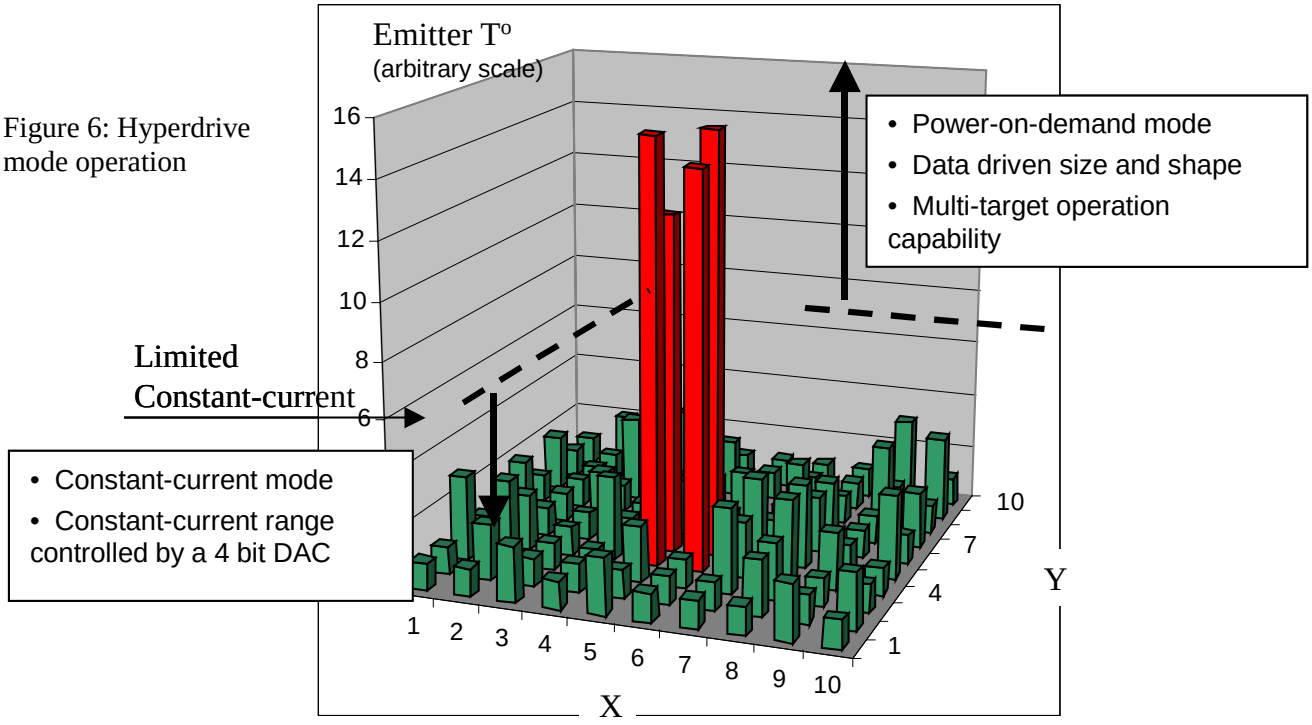


Figure 5: LAISE hyperdrive mode (background in constant-current mode and target in power-on-demand mode)

Figure 6: Hyperdrive mode operation



requirements. To operate a 1024 x 1024 array in *constant-current* mode (without *hyperdrive*) as in the MIRAGE 512 x 512 the RIIC would require nearly 500 Watts of cooling. By comparison, a 1024 x 1024 in *hyperdrive* mode with a constant current limitation corresponding to 400K apparent temperature, would require about 80 Watts of cooling (depending on the target temperature and size). The second benefit of *hyperdrive* is that it preserves much of the constant current immunity to electrical and thermal crosstalk. All emitter temperatures within the constant current regime will receive the full benefit of the *constant-current* mode.

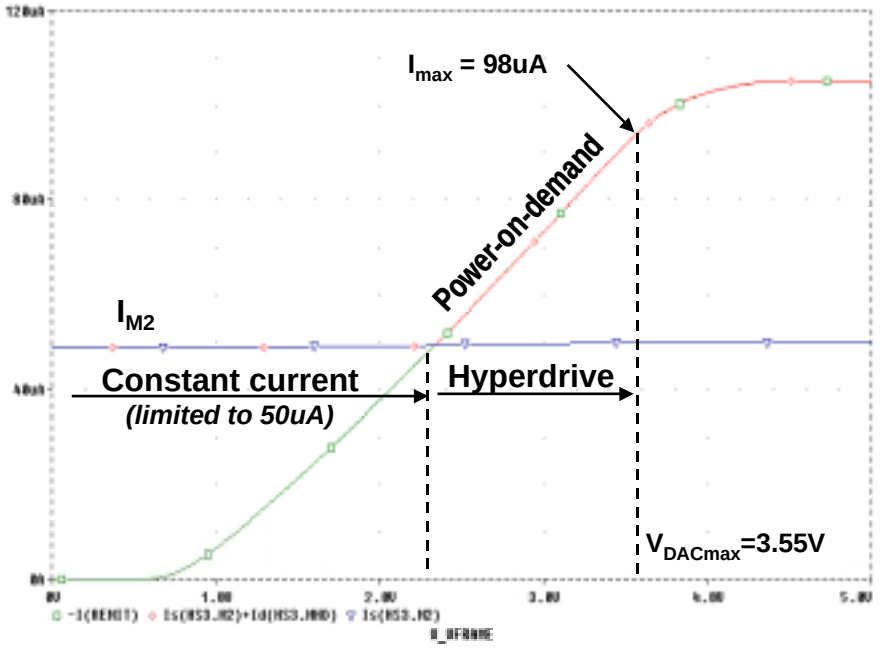


Figure 7: Simulation of the hyperdrive transfer function

The bus-bar robbing effect (seen in the *power-on-demand* mode) is greatly reduced in the *hyperdrive* mode. The target and background modes of operation being completely separated, a moving target will not generate any frame to frame crosstalk or dim after-image over the low temperature background. Different unit cell circuit configurations have been studied and compared against performance and real estate requirements. The *hyperdrive* configuration selected for the LAISE architecture is very simple and will be integrated with a minimum amount of additional real estate. The final unit cell size is expected to be less than 45 x 45 μm^2. The *hyperdrive* mode is triggered whenever the constant-current set for the background scene is reached. No additional control logic is required and the pixels in *power-on-demand* are simply defined externally by the input data level. The *hyperdrive* mode is therefore data driven, adding no special requirements on external electronics. Figure 6 is a representation of an array in the *hyperdrive* mode of operation. Figure 7 shows the simulation of the unit cell configuration chosen for the LAISE architecture, in the *hyperdrive* mode. It is anticipated that Non-Uniformity Correction (NUC) will be required for each user selected hyperdrive threshold (for each constant-current limit value).

4. Proposed LAISE Architecture

Eight 16-bit on-chip DACs, with adjustable offsets and dynamic range, will been implemented to generate the analog voltages corresponding to the emitter pixel radiance values. As scene data for one row is received, converted, and routed to appropriate column buffers (odd or even), the alternate set of buffers is writing the previous row of data up the column buses to individual unit cells.

At the end of a frame, when all 1024 x 1024 unit cell sample-and-hold capacitors are charged, the sample-and-hold capacitors are simultaneously connected to the input of the unit cell emitter driver. This process generates the next frame image.

The proposed LAISE unit cell architecture contains the programmable *constant-current*, *power-on-demand* and *hyperdrive* modes. In the *hyperdrive* mode, the background can be in *constant-current* mode while the data-driven target can be in *power-on-demand* mode. The *hyperdrive* mode allows a significant reduction of the power dissipation, depending on the temperature and size of the target over the background.

The large format RIIC emitter array requires high scene temperature dynamic range to allow the generation of hot targets (600K apparent temperature required for the MWIR band, up to 800K desired). A minimum frame to frame crosstalk, when a hot moving target is present over a cold background scene, is also desirable.

The proposed LAISE unit cell circuit has been designed to minimized frame to frame crosstalk and increase the instantaneous dynamic range. The increase in dynamic range allows for more efficient use of overdrive to correct for these effects. By overdriving (or under-driving) a pixel in the first frame of display where a transition occurs, it is possible to correct for the residual charge errors and reach the desired emitter temperature, based on an emitter's measured time constant. The LAISE unit cell transfer function is shown in Figure 8.

A maximum apparent temperature of about 700K has been measured on the first MIRAGE prototype with an emitter emissivity lower than the 70% predicted. Assuming 70% emitter emissivity, the desired dynamic range of 800K apparent temperature for the MWIR band is achieved with about 97µA emitter current. The LAISE enhanced dynamic range capability will give some margin for emitter output variations due to emissivity, emitter resistance or drive circuit variation from one emitter to another. It should be noted that the emitter material constraints would likely place a lower limit on the actual emitter apparent temperatures.

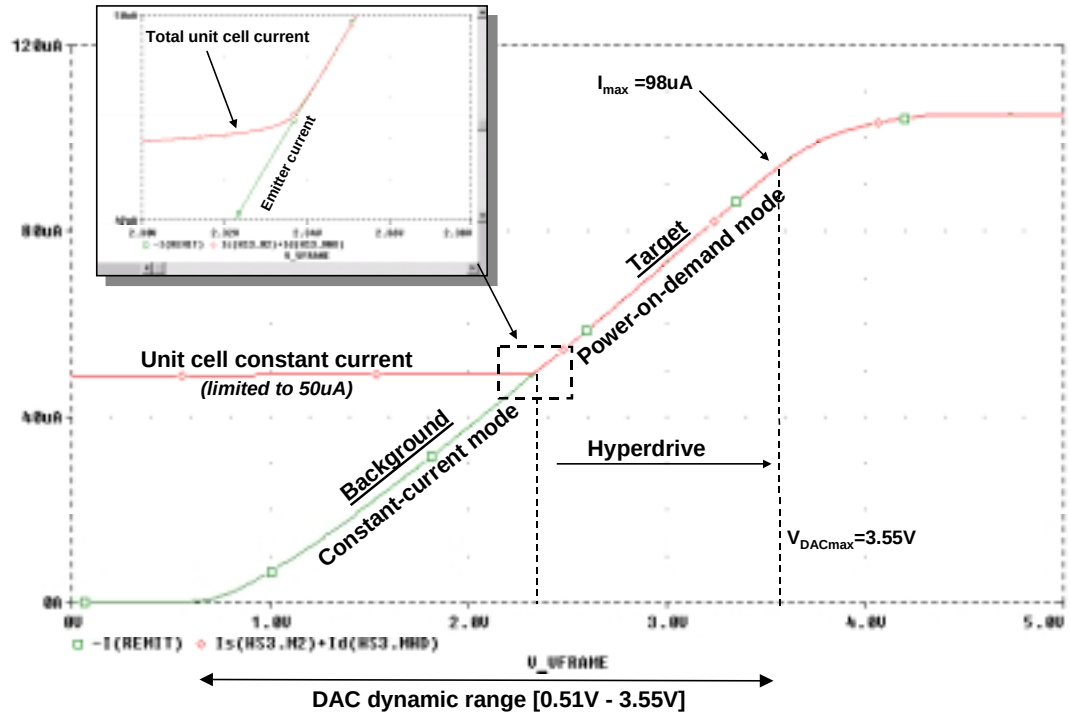


Figure 8: LAISE unit cell transfer function

5. UNIT CELL AREA CONSIDERATION

The final architecture to be implemented depends on the trade-off between the unit cell area and its performance. The MIRAGE unit cell uses 39 x 39µm^2 while the maximum dimension allowed for the LAISE unit cell is 45x 45µm^2, which corresponds to about 33% additional area. The unit cell will need to be modified and increased in size (from the MIRAGE unit cell 39 x 39µm^2) to implement the desired features (dynamic range enhancement, minimized frame to frame crosstalk and the *hyperdrive* mode).

Increasing the unit cell area results in lower substrate resistance and a proportional lower voltage drop across the substrate. In addition, an increased emitter fill factor is possible in the 45 x 45µm^2 design. However, a more complex design with larger pixels will result in a larger IC with potentially lower yield (although yields have been very high for the MIRAGE, therefore should be satisfactory for the larger LAISE array).

The LAISE RIIC will be implemented in the American Microsystems Incorporated (AMI), 5 volts, 0.5µm CMOS process (the MIRAGE RIIC was integrated in the AMI 0.6µm process). This process contains 5 layers of metalization allowing denser signal routing with lower impedance, reducing voltage drop in the supply lines. The AMI 0.5µm

process is also a planarized metalization process that will reduce the number of post-foundry processing steps required for emitter fabrication.

6. LAISE RIIC FABRICATION

Silicon integrated circuits use the process of photolithography to pattern device features such as transistors and wire interconnects onto the silicon wafer. Older CMOS fabrication processes, with minimum feature sizes of 1.0μm or greater, use masks the size of the entire silicon wafer, and the circuitry patterns of the entire wafer are exposed at one time. In this case, the maximum die size to be fabricated is limited only by the size of the silicon wafer.

Today, sub-micron CMOS processes are used due to their better performances in terms of speed, transistor and interconnection density (more than 3 layer of metalization) and wafer size 8'' to 12''.

Sub-micron processes use a method of exposure where a smaller optical field, or reticle, is stepped multiple times across the silicon wafer to expose the circuitry pattern of the entire wafer. Figure 9 shows examples of mask and reticle exposures. In this case, the maximum die size to be fabricated is limited by the size of the reticle field. A typical reticle field is approximately 20mm by 20mm. As the estimated die size for the LAISE RIIC is approximately 50mm by 50mm, it cannot be fabricated using conventional reticle stepping methods.

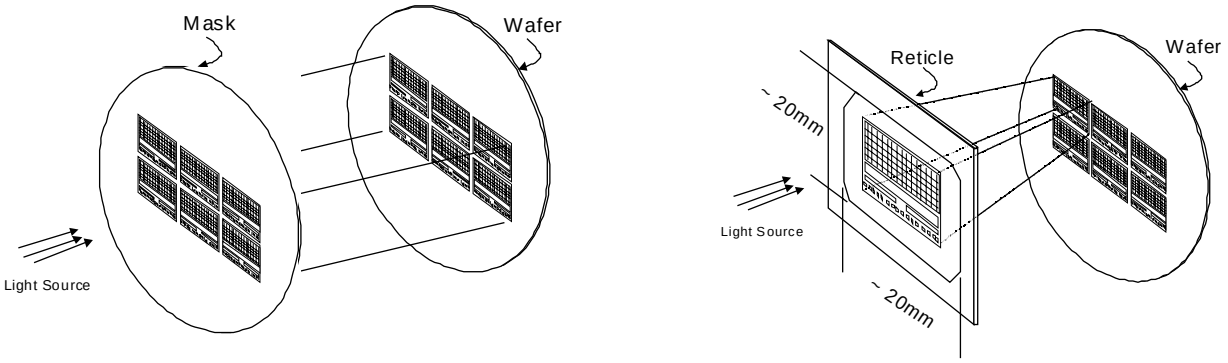


Figure 9: Mask and Reticle Exposure Examples

"Stitching" is a method used to allow fabrication of die larger than the reticle field. In this case, the die layout is divided into smaller portions, which together fit in the reticle field. Array characteristics or repeated sections of the die are exploited to minimize the required reticle area by using multiple exposures of smaller blocks to create a large array. Each die is then photocomposed on the wafer by multiple exposures of die sections at appropriate locations on the wafer. Single sections of the die are exposed at one time, as the optical system allows shuttering, or selectively exposing only a desired section of the reticle. Figure 10 depicts photocomposition of die on a wafer by stitching. It should be noted that stitching creates a truly seamless die, as opposed to assembly of closely butted pieces.

The LAISE 1024 x 1024 RIIC die is too large to be fabricated using conventional reticle exposure methods, and requires use of the stitching method. The die must be designed such that it can be composed of smaller pieces, and all of the required pieces must fit in the reticle field. The blocks must be designed such that they correctly abut adjoining blocks. Each portion of the die will be exposed individually, perhaps in multiple places, in order to compose a die exposure on the wafer.

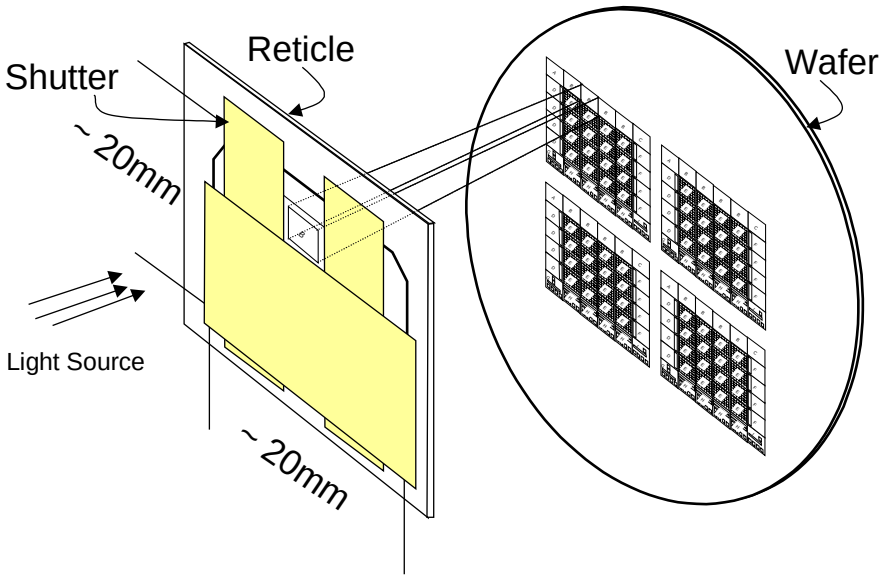


Figure10: Photocomposition of Die using Stitched Reticle

7. EMITTER FABRICATION

The LAISE 1024 x 1024 RIIC will be completely compatible with the existing Transfer Thin Film Membrane (TTFM) emitter fabrication process at Rockwell Science Center. The TTFM process allows initial emitter material processing to be performed independently from any RIIC processing. After emitter material and RIIC die have been partially processed, they are joined together in a step called mating. The TTFM process offers the advantages of wafer level emitter material annealing (prior to mating with the RIIC), and parallel processing of emitter material and RIIC die. In addition, reduced RIIC loss is realized by ensuring that only good emitter material is mated to known good RIIC die.

Currently existing production for MIRAGE emitter arrays (512 x 512) has employed mating and subsequent processing of two adjacent RIIC die, configured as a 2x1 rectangular block. Developmental mating of 2x2 blocks of four emitter arrays has been successfully demonstrated. Post mating processing steps can presently support materials sections as large as 5 inches in diameter. A 2x2 block of MIRAGE RIIC die will be only slightly smaller than the anticipated size of the LAISE 1024 x 1024 RIIC. Based on MIRAGE emitter processing experience, use of the TTFM process for future large format work is low risk.

8. PROPOSED LAISE PERFORMANCES

8.1 LAISE Performance Summary

The results of the LAISE architecture study showed that the Government and Industry requirements for the 1024 x 1024 emitter array can be achieved and implemented. The Large Area Infrared Scene Emitter will integrate all the required and desired functionality and performance identified for Government and Industry applications, with the exception of the dynamic windowing which will be implemented off-chip at the system level.

The emitter array will be externally controlled and programmed by a fully digital protocol for all its modes of operation including control of RIIC operating parameters such as bias adjustment. A full digital interface consisting of digital data inputs and digital RIIC control allows for much more operating flexibility by making all RIIC functions computer controllable and also greatly reduces the need for close support electronics. Most importantly, the all-digital interface removes the burden of placing low noise DACs as close as possible to the RIIC, resulting in a simplified emitter engine and greatly enhanced system noise immunity.

LAISE with its unique flexible power handling modes (*power-on-demand*, *constant-current* and *hyperdrive* modes) will allow end-user flexibility to determine the most useful power handling scheme to application specific trades. A fast static window running at 400 frames per second will allow future advanced high speed systems.

The LAISE RIIC has a very large dynamic range capability and presents a minimum frame to frame crosstalk improving the overdrive capability. LAISE pixel size is expected to be smaller than 45 x 45 μm^2, allowing trades between fill factor, emitter thermal mass (time constant) and total array size (yield) to be considered.

The TTFM process allows the emitter to be easily modified and mated to the existing RIIC, giving flexibility to the total system. Table 3 summarizes the functions and modes of operation to be implemented in the LAISE RIIC.

LAISE Modes of Operation	LAISE Function	Performance
All Digital Interface	▪ 8 DACs of 16 bit each	Digital input data (no external DAC, driving capability, system noise immunity)
	▪ Serial control register	RIIC parameters control (emitter current limit, constant current, DAC offset and range, main bias…)
	▪ tests	pixel characterization, DAC tests
Unit cell advanced circuitry	▪ Higher instantaneous dynamic range ▪ Minimized frame to frame crosstalk	higher apparent T^o can be reached increased overdrive capability smaller pixel size (smaller array)
Selectable Display Modes	▪ Rolling (or raster)	can be synchro with camera line time
	▪ Snapshot	stable images
Programmable Power Modes	▪ Power-on-demand	standard mode
	▪ Constant-current	no scene related crosstalk
	▪ Hyperdrive	low power operating mode no scene related crosstalk
Fast Static Window	▪ 1024 x 512 centered static window at 400 frames/sec	fast moving target lower emitter time constant capability
	▪ Background edges at lower frame rate	no window edge effect
On-chip temperature sensor	▪ Substrate temperature control	< 10mK accuracy

Table 3: LAISE performance summary

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