In order to achieve improvements in each of these metrics, development efforts within each subcomponent area are being pursued. New emitter pixels that leverage the basic design foundation of existing MIRAGE pixels, but incorporate new materials and geometries, have reached the program goal of 1500 K apparent temperature in the MWIR band (3.0 – 5.0 μm) during testing, corresponding to an in-band radiance of 2.47 W/cm^{2}sr. In addition, the design of a new read-in integrated circuit (RIIC) that will support a faster frame rate requirement of 500 Hz and the increased power required by higher temperature pixels has also been completed. The design of this RIIC supports array quilt packaging, in which multiple smaller RIIC tiles are packaged together to produce one composite larger emitter array. The first 3-side quiltable RIICs, which will verify key design elements of 4-side quiltable RIICs, have been fabricated and tested.

2. BACKGROUND AND GOALS

The UHT program calls for advancement in essentially every performance metric that characterizes a resistive array-based IRSP. This includes increasing the maximum MWIR apparent temperature from 700 K (0.13 W/cm^{2}sr) to over 1500 K (see Figure 1), increasing the maximum frame rate from 200 Hz to 500 Hz, and supporting array formats of up to 2048 x 2048 pixels. During the first phase of the program, emitter pixels incorporating new materials and geometries were fabricated and tested.[2] These pixels produced significantly more radiance than legacy pixels, and the data collected drove additional design modifications for the second program phase. In the second phase of the program, the material set for the pixel was refined based on the experiences from the first phase, and tested both in a bulk film anneal to over 1500 K and in individual test structures. Early second-phase pixels incorporated improvements in photolithography (resulting in improved fill factor) and geometric designs that had been identified by finite element analysis (FEA) as likely to respond best to thermo-mechanical stress. The first batch of pixels tested in this phase approached the program goal of 1500 K, and improved upon the MWIR radiance of legacy designs by a factor of nearly 20x.[3]

After the large-array trade study confirmed QP as the optimal path to larger and faster emitter array formats, a new read-in integrated circuit (RIIC) design was initiated and completed.[3,4] This baseline design consists of a 512 x 768 tile size built up from modular stitch blocks, and incorporates QP nodules on 3 of its 4 sides. The fourth side features conventional bond pads for signal input/output, while power and ground are routed through the backside via TSV's. RIICs using this design will be used as tiles to build a scalable array with N x 512 columns and up to 1536 rows (N x 2 tile format), and thus will provide an effective platform for testing the technologies that will ultimately be used to produce 4-sided quiltable RIICs for even larger array formats. SEM imagery of test designs confirmed that sub-pixel alignment and spacing between tiles can be achieved, which will prevent artifacts in the projected imagery at the tile boundaries. Simulations performed on the 512 x 786 RIIC design confirmed that the RIIC can achieve the desired 500 Hz frame rate and deliver up to 3.2 mW per pixel. With the current configuration that relies on TSVs for power routing, the design is expected to achieve a spatial power variation of less than 1%, even with a significant fraction of the array driven to maximum power.

[4] Sparkman, Kevin, LaVeigne, Joe, McHugh, Steve, Kulick, Jason, Lannon, John, Goodwin, Scott, "Scalable Emitter Array Development for Infrared Scene Projector Systems", Proc. SPIE 9071, (2014)

[5] LaVeigne, Joe, Franks, Greg, Danielson, Tom, “Thermal Resolution Specification in Infrared Scene Projectors”, Proc. SPIE 9452 (2015)